Structural Isolation in Circuit Optimization

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Structural isolation, where functionally similar logic components are dispersed or obscured within a circuit, hinders both optimization and hardware security. The study employed DeepGate, a graph neural network (GNN) trained to generate joint structural and functional embeddings of circuit elements. Using Euclidean distance between embeddings, DeepGate identifies and rewires isolated yet equivalent logic. Experiments on ISCAS-85 benchmarks show that logic-preserving transformations, such as inverter insertions and De Morgan rewrites, produce minimal embedding drift, confirming robustness to structural noise. In contrast, cosine similarity was overly sensitive, with small edits triggering disproportionate changes, making it unreliable for fine-grained analysis. These findings suggest that DeepGate encodes circuits in a compact yet nuanced space, although its limited ability to distinguish distinct circuits indicates a potential representation bottleneck. The study is now focused on PolarGate, a GNN that incorporates polarity-aware message passing and contrastive training. Leveraging structured perturbations as examples, the current work aims to develop more accurate and discriminative embeddings for improved circuit analysis and synthesis.

Introduction

Structural isolation refers to cases where functionally similar logic components in a circuit are structurally separated or hidden, making them hard to identify as equivalents. This becomes a problem because functionally identical subcircuits may remain unmerged, missing key optimization opportunities. Security-critical logic may also become isolated, making it more vulnerable to removal or attack. This challenge has implications for hardware security—such as preventing hidden security gates from being pruned—and for functional similarity detection, including the identification of IP core reuse or Trojans in obfuscated circuits. Traditional cut-based optimization methods struggle to detect these functionally similar but physically distant components, limiting both performance and design security. Addressing structural isolation requires a way to recognize functionally alike structures despite different layouts.

DeepGate Graph Embedding Approach

This work utilizes DeepGate, a graph neural network (GNN) model, to generate vector embeddings for logic gates within a circuit. Each node (gate) is encoded in a high-dimensional space that captures its structural context and logical function. The DeepGate model is trained with a combined structural and functional objective, ensuring that gates performing similar logical roles produce similar embeddings, even when they are distant in the circuit graph. This design enables the model to effectively integrate structural and functional information by learning from both the connectivity among gates and their logical behavior, using examples that emphasize both types of similarity (1). After training, the Euclidean distance between node embeddings serves as a quantitative similarity metric (2). This metric guides subsequent circuit transformations by identifying isolated yet similar logic. In practice, the optimization algorithm selects nodes from structurally isolated regions that exhibit minimal embedding distance to one another and then merges or rewires these nodes to reduce isolation.

Experimental Findings and Observations

DeepGate's embedding-based optimization was evaluated on standard logic benchmarks (e.g., the ISCAS-85 circuits). Several structural experiments were conducted to test the embedding's sensitivity. For example, logically neutral inverter pairs were inserted, or De Morgan's law transformations were applied to alter the gate structure without changing the output function (3). In each case, the modified circuit's embedding remained highly similar to the original; only a modest increase in Euclidean distance was observed, indicating that DeepGate's embeddings correctly recognized the circuit as largely the same logic.

Conversely, experiments using a cosine-similarity metric exposed an undesirable sensitivity: adding only a few gates caused both structural and functional cosine distances to spike disproportionately. Such volatility suggests that the angular metric over-amplifies minor edits and may be ill-suited for reliable, fine-grained circuit analysis. These results suggest that the embedding space captures fine differences but remains compact. Small functional or structural changes lead to only slight shifts in the learned vector space, and even distinct circuits inhabit a relatively close neighborhood. In other words, DeepGate's embedding metric encodes circuit characteristics in a compressed form, where differences are present but within a narrow range. This compact similarity space implies that a more expressive embedding model is needed for synthesis tasks.

Benchmark	Method	Output	Struct Dist	Func Dist	Struct Sim	Func Sim	Time (s)
c17	demorgan	po1	0.0085	0.0024	0.18	0.83	2.2
c17	demorgan	po1	0.00045	0.00041	0.99	1.0	2.1
c17	compare	po0	0.00038	0.00027	1.0	0.99	3.0
c17	compare	po0	0.00040	0.00023	0.99	0.99	2.2
c432	demorgan	po0	0.0071	0.0011	0.92	0.71	3.5
c432	demorgan	po0	0.00051	0.00053	1.0	1.0	3.8
c432	compare	po2	0.00072	0.00022	1.0	1.0	15
c432	compare	po2	0.00026	0.00010	1.0	1.0	14
c3540	demorgan	po02	0.017	0.012	0.42	0.87	5.3
c3540	demorgan	po02	0.00062	0.00037	1.0	1.0	5.3
c3540	compare	po10	0.00810	0.0020	0.65	0.11	16
c3540	compare	po10	0.00051	0.00051	1.0	0.5	32
c5315	demorgan	po081	0.020	0.018	-0.071	-0.83	13
c5315	demorgan	po081	0.00029	0.00026	1.0	1.0	16
c5315	compare	po102	0.00620	0.00480	0.53	-0.88	17
c5315	compare	po102	0.00026	0.00027	1.0	1.0	31

Table I: *Euclidean structural and functional distances for representative ISCAS-85 benchmarks following baseline comparison and De Morgan rewrites.* *DeepGate embeddings primarily exhibit smaller functional than structural distances, and run-time measurements confirm feasibility for in-flow optimization.*

Conclusion and Future Work

The results demonstrate that GNN-based embeddings can successfully identify and guide the consolidation of functionally similar logic in circuits, assisting in overcoming structural isolation for optimization. The embedding-driven method maintained functional correctness while reducing isolated logic structures, indicating promising directions for ML-guided EDA tools. However, the compactness of the DeepGate embedding space and the unexpectedly small distances between dissimilar circuits highlight a potential functional representation bottleneck. To address this, the research now focuses on exploring PolarGate as an alternative embedding approach. PolarGate is a recently proposed GNN technique that introduces polarity-based node embeddings and differentiable logic operators to better capture logical functionality in circuits. By leveraging positive and negative signal representations and enriched message passing, PolarGate is expected to generate embeddings that more distinctly separate circuit functionalities than DeepGate, producing a more accurate similarity metric. Using this improved discrimination, the study incorporates a library of controlled structural and functional perturbations—such as inverter-pair insertions and De Morgan rewrites—as contrastive examples in future training rounds, further enhancing the model's fidelity to meaningful design differences.

REFERENCES

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Ivan Byju is a third-year undergraduate student studying computer engineering, with minors in computer science and business. Since Fall 2024, he has been engaged in research on DeepGate, a graph-embedding framework for circuit security. His work explores the intersection of hardware design and machine learning, focusing on structural isolation and similarity measures. Beyond research, Ivan has a strong interest in computers and technology and enjoys staying at the forefront of innovation in AI and engineering. This project has broadened his understanding of how advanced algorithms can address challenges in electronic design automation and security, further fueling his passion to push boundaries in impactful ways.

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Dr. Kyle Juretus is an assistant professor in the Electrical and Computer engineering department at Villanova University. He received his Ph.D. in Electrical Engineering from Drexel University in 2020. During his Ph.D. studies, Dr. Juretus was a National Defense Science and Engineering (NDSEG) fellow sponsored by Air Force Research Laboratory (AFRL) from 2016-2019. His research focuses on Integrated Circuit (IC) design with the objective to create faster, smaller, more efficient, and more secure ICs. To enable such changes with minimal design time overhead, Dr. Juretus focuses on the development of next generation electronic design automation (EDA) tools.