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IMPLEMENTATION OF DIGITAL SIGMA-DELTA MODULATORS FOR HIGH-RESOLUTION AUDIO DIGITAL-TO-ANALOG CONVERTERS BASED ON FIELD PROGRAMMABLE GATE ARRAY

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Sigma-delta modulators (SDMs) are now widely used in high-resolution audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The field programmable gate array (FPGA)-based hardware is particularly suitable for the implementation of basic functional blocks of audio sigma-delta DACs. This paper presents the design, simulation, and the FPGA implementation of the lowpass digital sigma-delta modulators (SDMs) in various configurations. The results can be used for digital SDM designs and its future applications in the audio sigma-delta DACs as well as for educational purposes.

Keywords: Audio Sigma-Delta DAC, Digital sigma-delta modulator, FPGA.

1. Introduction

An audio digital-to-analog converter (DAC) is a key element of every CD/DVD player system. Recently, sigma-delta DACs (also known as oversampled noise-shaping DACs) have become an attractive alternative to conventional R-2R DACs (Nyquist rate PCM or oversampled PCM) mainly in the consumer, but also in professional audio playback systems [1]. They offer high resolution and low distortion with relaxed post-analog filter requirements at a relatively low cost, compared to conventional laser-trimmed R-2R DACs.

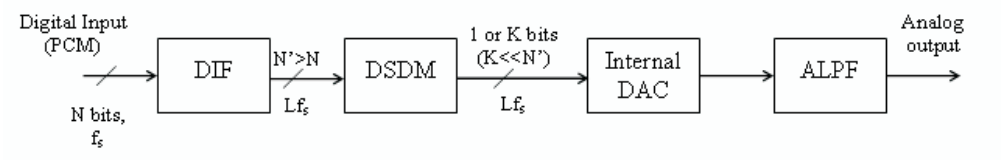

Fig. 1. Block diagram of a typical sigma-delta DAC.

A typical sigma-delta DAC, shown in Fig. 1, consists of a digital interpolation filter (DIF), low-pass digital sigma-delta modulator (DSDM), internal (core) DAC, and analog low-pass post-DAC filter (ALPF).

The DIF performs upsampling of a multi-bit digital input signal, that is, a stream of $N-$bit words with a sampling rate of f_S (usually, f_S is slightly greater than the Nyquist rate of the signal) changes to a stream of $N'-$bit words (usually, $N' > N$) with a sampling rate of Lf_S, where L is the oversampling ratio. The DSDM shortens the word length to K bits (usually, $K << N'$) or to a single bit and spectrally shapes the truncation noise which can be viewed as pushing noise power from the signal band to higher frequencies. The truncated output signal of the DSDM (i.e., a K- or a 1-bit data stream with a rate of Lf_S) is converted by the internal DAC. Finally, the analog output of the internal DAC is fed to the ALPF for the out-of-band noise filtering and the analog signal reconstruction. In high oversampled 1-bit (two-level) sigma-delta DACs, the modulators with 1-bit requantizers (truncators) and the inherently linear 1-bit internal DACs are used. These converters, however, create problems, such as high amount of truncation noise and the increased clock-jitter sensitivity. Usually, a complex post-DAC filter is required to attenuate the out-of-band truncation noise to acceptable level. During the last decade, low-bit (multi-level) sigma-delta DACs have become popular. Compared to 1-bit converters, the advantages of low-bit converters are an increase in the stability and performance of modulators, the reduction of the required oversampling ratio, less susceptibility to idle tones and the reduction of the out-of-band truncation noise, thereby relaxing the requirements of the post-DAC filter. The disadvantage is low-bit internal DAC nonlinearity, which is the cause of the analog elements mismatch. This problem can be solved using dynamic element matching (DEM) , e.g., based on the second-order data weighted averaging (DWA) algorithm [2].

The most important audio DACs (also ADCs) specifications are signal-to-noise ratio (SNR), dynamic range (DR) and total harmonic distortion plus noise (THN+N). Typically, a high performance sigma-delta audio DAC should have 110-120 dB SNR (or DR) and 100-110 dB THD+N. Commercially available sigma-delta audio DAC chips are produced in the submicrone CMOS VLSI technology. However, sometimes the FPGA technology is very suitable for constructing high-performance digital signal processing (DSP) systems as well as FPGA-based hardware such as audio sigma-delta DACs, which are primarily digital systems. FPGAs also make an excellent prototyping environment for the sigma-delta DAC designs, for example in a digital audio signal processing laboratory for students [4].

In the paper, the design, simulation and implementation of four chosen structures of DSDMs using FPGA technology is presented as a limited task. These modulators are designed to be used in high-resolution audio sigma-delta DACs.

2. Basic configurations of single-loop DSDMs

The DSDM is a crucial part of a sigma-delta DAC, likewise the analog SDM (ASDM) is of a sigma-delta ADC. DSDMs can be classified by the order, the configuration

(single-loop or multi-stage noise shaping) and the type of the feedback signal (most significant bit or least significant bit's/error feedback). Multi-stage noise shaping (MASH) or cascaded DSDMs are beyond the scope of this paper, so only single-loop DSMD configurations will be considered.

There are two basic configurations of single-loop DSDMs. The first configuration of a single-loop 1-bit DSDM with the most significant bit (MSB) feedback is shown in Fig. 2a. It consists of a low-pass filter (loop filter) with transfer function $H(z)$and a requantizer (truncator) which cuts off the MSB. The MSB is the negative, fed back to the input and output to the internal 1-bit DAC. Because DSDMs are nonlinear systems, in order to derive a linear model of a DSDM, the truncator is modeled as a summing node with additive white truncation noise $E(z)$.

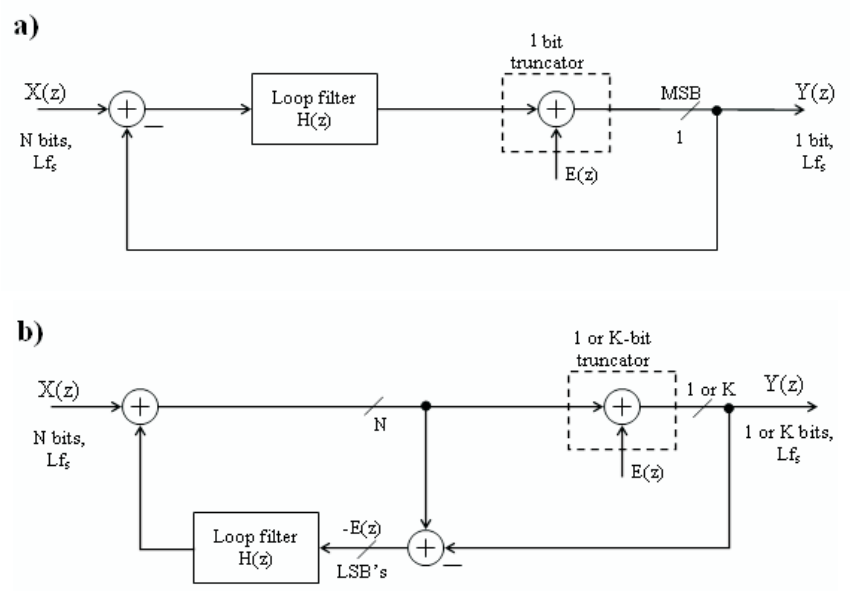

Fig. 2. The block diagrams of single-loop DSDM configurations: a) 1-bit modulator with MSB feedback, b) 1- or K-bit modulator with LSB's error feedback.

A useful alternative to a digital noise-shaper loop with the MSB feedback is a so-called error feedback configuration shown in Fig. 2b. In this configuration, instead of the MSB output, the negative of truncation error $E(z)$, i.e., the least significant bit's (LSB's), is fed back to the input through the loop filter with the transfer function $H(z)$. The stream of digital words with a word length of 1 bit or K bits (i.e., the MSB's) and data rate Lf_S is sent to the internal DAC.

In z-domain the loop filter $H(z)$ can be characterized with signal transfer function $H_S(z)$ and noise transfer function $H_{NS}(z)$. It means that the DSDM acts as a low-pass filter for the signal and a high-pass filter for the truncation noise, shaping the noise in such a way that a high proportion of the noise energy is contained above the audio signal bandwidth. Simple analysis shows that output $Y(z) = H_S(z)X(z) + H_{NS}(z)E(z)$ is the

superposition of input signal $X(z)$ and noise signal $E(z)$ transformed by the system. In the simplest case, the low-pass filter (loop filter) may be merely an accumulator with a transfer function of $H(z) = z^{-1}/(1 - z^{-1})$ *= 1/(z – 1)* or *H(z) = 1/(1 –* z^{-1}*) = z/(z – 1),* resulting in the first order noise-shaping with noise transfer function H_{NS}*(z) = 1 –* z^{-1}. The noise transfer function for the $R-$order noise-shaping is H_{NS}*(z) = (1 –* z^{-1}*)*^{R} , i.e. the $H_{NS}(z)$ is the $R-$order high-pass function. It may be stated that the higher the order of a loop filter is, the greater becomes the SNR in-band (with the penalty of increased out-of-band truncation noise power) for a given oversampling ratio L. In a single-loop architecture, the order of a modulator is determined by the number of noise-shaping stages within the loop. Additionally, the higher order modulators provide significant improvements in the DR performance and the reduction of idle tones. However, it is possible to use digital dithering to prevent the generation of tones in any of the DSDM configurations. Since the noise-shaping loop in a DSDM is a pure digital circuit, the stability of the loop can be assured even if the loop filter order is high. There is a number of the loop filter configurations which can realize higher order noise transfer functions.

3. The proposed DSDM configurations and spectral simulation results

In our design, four single-loop DSDMs are proposed in two re-configurable structures [2, 3]. The first two are based on the MSB feedback structure which can be configured as either 3rd order or 5th order 1-bit modulators. The other two are based on the LBS's error feedback structure which can also be configured as either 3rd order or 5th order 5-bit modulators. Figures 3 and 4 show the block diagrams of the proposed structures. Each structure is configured as a 5th order one, with all the shadowed blocks active. If the shadowed blocks are omitted, then the structures become the 3rd order. The structure shown in Fig. 3, known as a cascade-of-resonators feedback form (CRFB), can be arranged with different combinations of coefficients g[i] equal to zero, which means that those paths are removed from the structure. In this way, the 3rd order noise-shaper consists of a cascade of an accumulator and a resonator, and the 5th order noise-shaper consists of a cascade of an accumulator and two resonators.

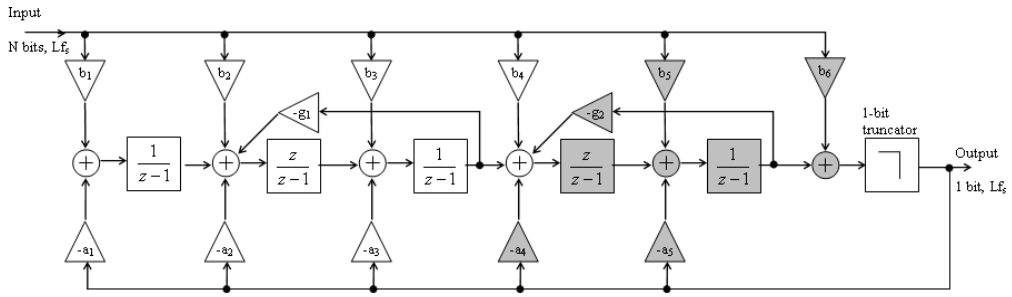

Fig. 3. Structure of the re-configurable 3rd/5th order DSDM with MSB feedback.

Table 1. Coefficients of 1-bit DSDM.

Structure			
	3rd order	b[i]	0.0441 0.2431 0.05559 1.0000
		g[i]	0.0014 0.0000
		a[i]	0.0441 0.2431 0.5559
	5th order	b[i]	0.0007 0.0087 0.0554 0.2502 0.5562 1.0000
		g[i]	0.0070 0.0020
		a[i]	0.0007 0.0087 0.0554 0.2502 0.5562

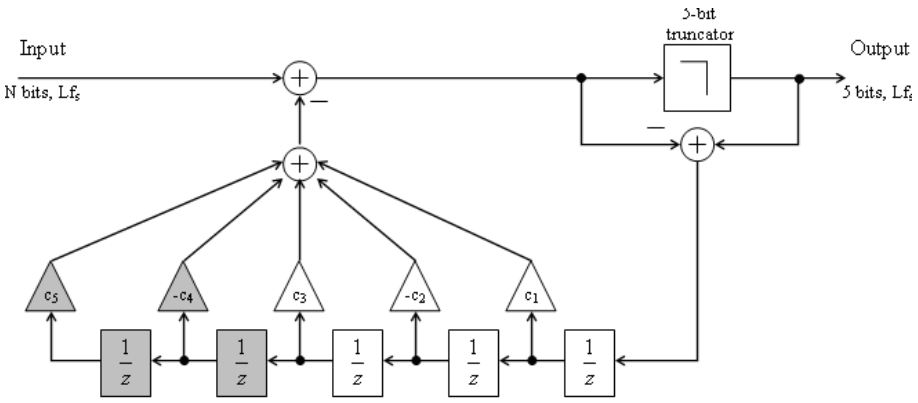

Fig. 4. Structure of the re-configurable 3rd/5th order DSDM with LSB's error feedback.

Table 2. Coefficients of 5-bit DSDM.

Structure			
	3rd order	c[i]	3 3 1
	5th order	c[i]	5 10 10 5 1

The coefficients b[i], g[i], a[i] and c[i] of the proposed DSDMs were obtained in the Matlab environment [5] using the *delsig* toolbox. The values of coefficients are given in Tables 1 and 2. For simulation purposes, the original sampling frequency f_S = 44.1 kHz, the oversampling ratios L_1 = 64 and L_2 = 128 which give the input data rates of 2.8224 MHz and 5.6448 MHz, and the sinusoidal input signal with an amplitude of 0.5 (i.e. half of the full scale range) were assumed.

Figure 5 shows the output spectra for the re-configurable 3rd/5th order structure of the modulator depicted in Fig. 3, at the oversampling ratios L_1 and L_2 respectively. Under the 3rd order structure, the maximum SNR of the modulator within the audio band is about 83 dB at L_1 and about 101 dB at L_2. Only the second value of the SNR

is sufficient for the 16-bit data. Under the 5th order structure, the maximum SNR of the modulator within the audio band is about 108 dB at L_1, which is sufficient for the 16-bit data, and about 141 dB at L_2, which is sufficient for the 18-, 20-, and 24-bit data. The effects of the higher oversampling ratio and notches introduced by the resonators are clearly visible, which results in the improvement of the SNR performance. Since the idle tones are not present, there is no need to use the dithering.

Figure 6 shows the output spectra for the re-configurable 3rd/5th order structure of the modulator depicted in Fig. 4. Under the 3rd order structure, maximum SNRs in the audio band are about 124 dB and 144 dB at L_1 and L_2 respectively. The first value of the SNR is sufficient for the 18- and 20-bit data, and the second one for the 18-, 20-, and 24-bit data. Under the 5th order structure, the obtained maximum values of the SNRs are 154 dB and 187 dB at L_1 and L_2 respectively. These last values of the SNRs are excessive for the 24-bit data conversion systems, so the required oversampling ratio can be reduced to $32\times$ or even to $16\times$, depending on the application. Also in this case, there is no need to use dithering.

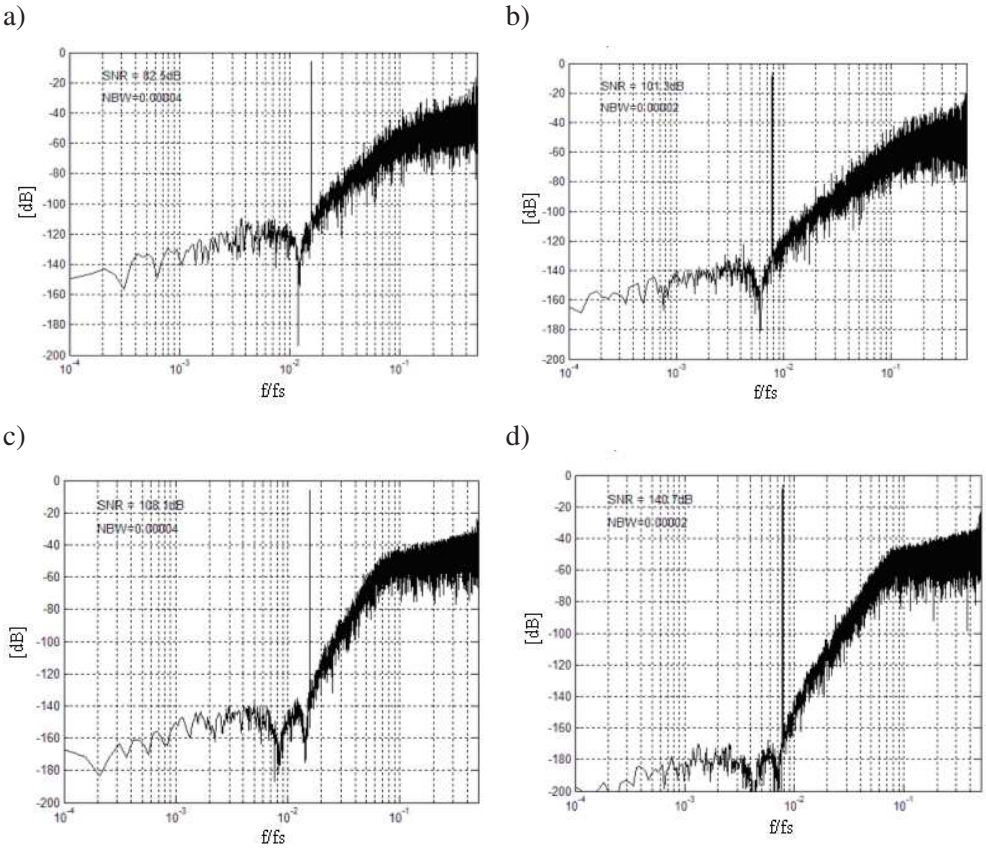

Fig. 5. Simulated output spectra of the 1-bit modulator; a) 3rd order, $f = f_S/64, L_1$; b) 3rd order, $f = f_S/128, L_2$; c) 5th order, $f = f_S/64, L_1$; d) 5th order, $f = f_S/128, L_2$; $L_1 = 64, L_2 = 128$.

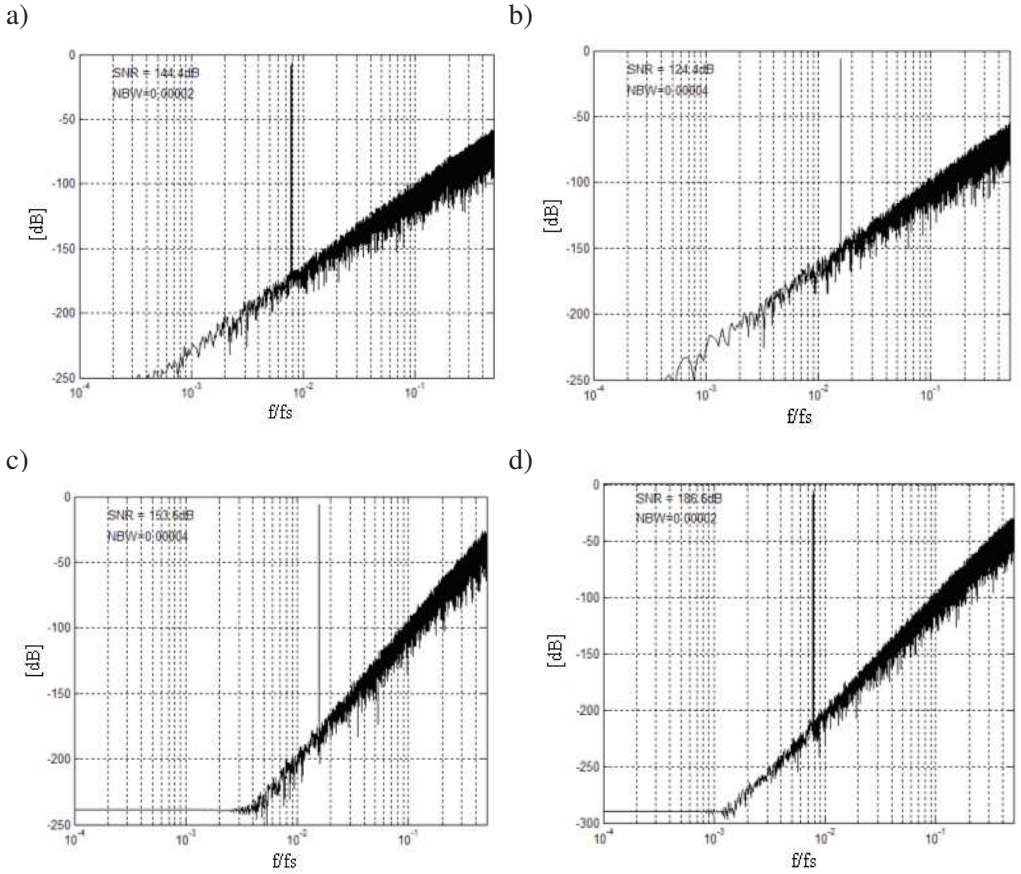

Fig. 6. Simulated output spectra of the 5-bit modulator; a) 3rd order, $f = f_S/64, L_1$; b) 3rd order, $f = f_S/128, L_2$; c) 5th order, $f = f_S/64, L_1$; d) 5th order, $f = f_S/128, L_2$; $L_1 = 64, L_2 = 128$.

4. FPGA-based prototyping platform and experimental results

The Altium LiveDesign development board, as the prototyping platform which embeds the Altera Cyclone EP1C12F324 FPGA chip, was selected for the implementation of the DSDMs presented in the previous section. The FPGA chip was directly programmed from the PC using a parallel interface (according to the JTAG standard) to transfer the data and the Altera Quartus II software. In the case of the 1-bit 3rd and 5th order modulators, the coefficients were rounded off due to the finite precision without any significant influence on the output noise-shaped spectra. Additionally, the multipliers were replaced by the multiplexers.

The measurements of the modulators implemented in the Cyclone FPGA chip were performed using the SignalTap II Logic Analyzer tool included in the Quartus II software. Because of the limited volume of the Cyclone internal memory, only the 65522

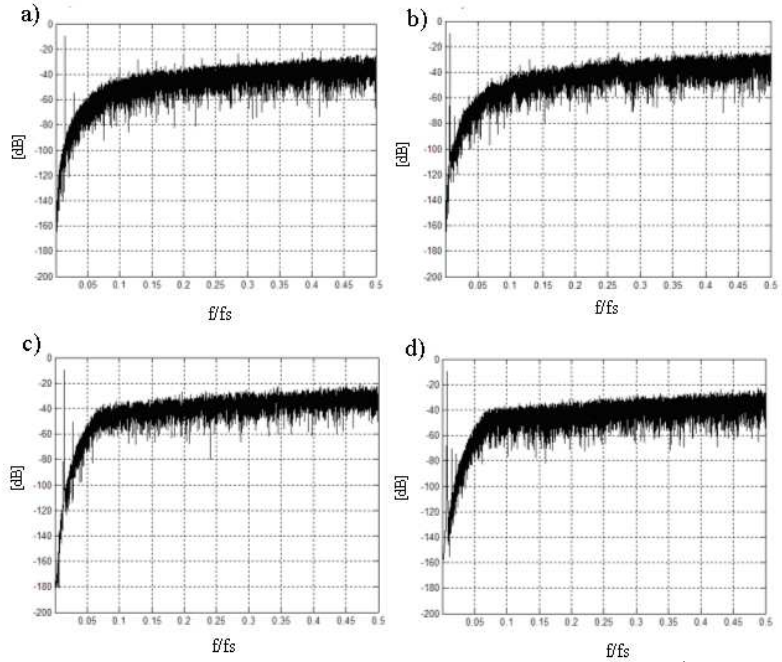

Fig. 7. Measured output spectra of the 5-bit modulator: a) 3rd order, $f = f_S/64$, L_1; b) 3rd order, $f = f_S/128$, L_2; c) 5th order, $f = f_S/64$, L_1; d) 5th order, $f = f_S/128$, L_2; $L_1 = 64$, $L_2 = 128$.

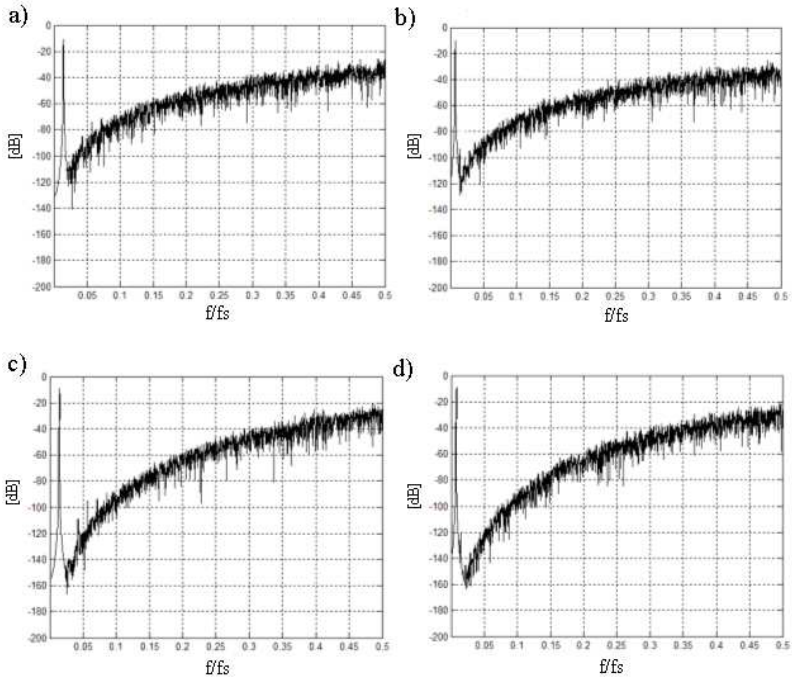

Fig. 8. Measured output spectra of the 5-bit modulator: a) 3rd order, $f = f_S/64$, L_1; b) 3rd order, $f = f_S/128$, L_2; c) 5th order, $f = f_S/64$, L_1; d) 5th order, $f = f_S/128$, L_2; $L_1 = 64$, $L_2 = 128$.

samples for 1-bit modulators and 8192 samples for 5-bit modulators were taken. The sinusoidal input signal with the amplitude of 0.5 was used. Figures 7 and 8 show the measured output spectra.

As can be seen, the measured spectra are comparable with the spectra obtained from the simulations. Only in the case of the 1-bit 3rd order modulators, the measured spectra contain some tonal distortion which can be eliminated using the low-level digital dithering.

5. Conclusions

In this paper, we have presented the design and implementation of two types of re-configurable DSDMs on the FPGA platform. With different modulator orders, it is possible to achieve different SNRs for various audio sigma-delta DACs applications. Finally, it has been shown, that an FPGA-based platform creates very useful prototyping environment for the implementation and testing of the DSDMs.

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