Design, characterisation, and digital linearisation of an ADC analogue front-end for gamma spectroscopy measurements

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ABSTRACT
This work presents the design, experimental characterisation, and digital post-distortion (i.e., digital linearisation) of a MHz-range ADC analogue front-end prototype for a gamma radiation spectrometry system under development at the National Center for Nuclear Research (NCBJ) in Poland. The design accounts for the electrical response of the gamma particle detector in providing signal conditioning and ADC protection against high-voltage spikes due to occasional high-energy cosmic radiation, as well as proper ADC clocking. As the front-end inevitably introduces nonlinear distortion and dynamic effects, a characterisation is performed to quantify the actual performance in terms of Total Harmonic Distortion (THD) and Effective Number of Bits (ENOB). Thus, a digital linearisation based on both static and memory polynomial models is successfully applied by means of post-distortion processing, guaranteeing a substantial improvement in THD and ENOB, and demonstrating the effectiveness of the hardware/software method for gamma radiation spectrometers.

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1. INTRODUCTION

Gamma spectroscopy is the discipline studying gamma radiation sources. The identification and characterisation of gamma radiation sources is employed for many purposes, ranging from scientific to industrial, as well as military. In geology, it can be employed for mapping the elements in rock formations (mainly potassium, thorium, and uranium) [1], or for analysis of soil samples [2]. In border security, non-intrusive inspection systems based on gamma spectroscopy can detect materials such as tobacco, illicit drugs, or explosives [3]. Also, gamma spectroscopy systems are commonly used for radiation monitoring, e.g., they are always found near sensitive nuclear apparatuses such as nuclear reactors or particle accelerators. In case of a fault, any radiation exceeding predetermined safe levels can be quickly detected, triggering the shutdown of the system and corresponding actions.

Gamma spectroscopy measurements aim at quantifying the energy of radiated particles. The energy spectrum of such radiation can be experimentally obtained by creating a histogram of the energy levels. Then, the peaks in the spectrum can be related to specific physical processes happening at the atomic scale, granting insights into the nuclear composition of a measured source of radiation.

A gamma spectrometer consists of an ionising radiation detector and an electrical signal receiver. The detector converts the radiation energy of the incoming particles into voltage pulses, the pulse amplitude being proportional to the energy of the particle. Legacy spectrometry systems consist of several modular elements, such as charge-sensitive pre-amplifiers and pulse-shaping filters, to increase pulse duration and make it suitable for the Analogue-to-Digital Converter (ADC). In modern systems, instead, the use of fast ADCs allows to minimise signal conditioning, enabling direct pulse sampling, higher pulse count rate, and a reduced risk of *pulse pile-up* [4]. After the acquisition,

the captured voltage pulses must be integrated in time to quantify the particles energy, and the accuracy of the estimated energy spectra heavily depends on the receiver performance.

A fundamental problem in spectrometers is the occasional presence of high-energy cosmic radiation interfering with regular acquisitions. Most critically, the voltage spikes resulting from these rare events can have amplitudes an order of magnitude higher than the typical radiation source. Since the acquisition system of spectrometers is normally designed to maximise measurement sensitivity and accuracy, the output signal of the detector is normally set to match the ADC dynamic range with the typical amplitudes received from the target radiation, usually in the few volts range. Therefore, the unwanted cosmic pulses can take amplitude of tens of V, not only saturating but even damaging the ADC. In this context, ADC protection from the high-voltage transient events becomes a system pre-requisite. In legacy spectrometers, this protection is indirectly provided by the pre-amplifier. In direct sampling systems, instead, such protection can be obtained by introducing analogue signal limitation yet paying attention to preserve good receiver linearity within the dynamic range of the ADC. More precisely, both the necessary signal conditioning and the analogue limiter itself will likely introduce dynamic effects and nonlinear distortion, reducing the receiver dynamic range.

The characterisation and correction of ADC-based receiver non-idealities has been subject of extensive research in the literature [5]-[9]. In particular, digital linearisation is an effective approach for compensating the nonlinear dynamic distortion caused by hardware [7]-[9]. It consists of the extraction of a suitable mathematical description of the nonlinear dynamic behaviour of the device, often derived from Volterra-like series representations [9]-[12]. This mathematical model is extracted through a set of measurement procedures, either using time or frequency domain approaches. Once a suitable direct model of the device is extracted, linearisation can be performed by implementing an inverse of the identified model using digital signal processing techniques. Whereas this process is known as digital pre-distortion when linearising signal generators, transmitters, or power amplifiers [13], [14], it can be implemented as *Digital Post-Distortion* (DPD) for receivers by applying the inverse model to the corrupted samples acquired by the digitiser [8], [15]-[17].

In this work, we present the design, characterisation, and digital linearisation of an ADC analogue front-end for the gamma spectrometry system under development at the Polish National Centre for Nuclear Research (NCBJ). Such a board prototype implements a tailored signal conditioning stage including the ADC protection and it hosts the clock generation for the ADC, as well as all the necessary ADC control hardware. This article extends the one in [18], presented at the 24th IMEKO TC-4 International Symposium and 22nd International Workshop on ADC and DAC Modelling and Testing. The conference contribution was mainly devoted to the metrological characterisation of the front-end in a laboratory setting, and to investigate the feasibility of digital linearisation approaches with application-like pulsed waveforms. In this work, we provide a presentation of gamma spectroscopy systems, in particular targeting the one under development at NCBJ. Moreover, we present the design details for signal conditioning, especially for the on-board reference clock and the assessment of its jitter. For both aspects, new characterisation data is provided. Also, we describe the hardware components of the designed front-end

board. Finally, the proposed spectrometry system is tested in field using an actual gamma radiation source (Caesium-137).

The article is organised as follows. In Section 2, the working principles of the gamma spectrometer are provided. Section 3 is dedicated to the design of the analogue front-end prototype, including the signal conditioning stage and ADC reference clock. Section 4 contains the corresponding characterisation performed to verify the suitability of the design. Moreover, it reports the metrological characterisation of the front-end both with the standard-compliant method using sine wave excitations, as well as using pulsed signals typical of gamma spectroscopy applications. In Section 5, the DPD approach is successfully implemented, substantially improving the linearity performance of the receiver protected by the front-end. In Section 6, the characterisation of the front-end in an actual spectrometry system is carried out and DPD is applied in the real-life setting. The effects of the distortion and linearisation are presented for measuring the energy spectrum of Caesium-137. Conclusions are drawn in Section 7.

2. GAMMA SPECTROSCOPY SYSTEM

A fundamental part of a gamma spectrometer is the detector of gamma radiation. The most used type of detector, suitable for a wide assortment of radiations, is the scintillation detector [4]. Its working principle is based on *scintillation*, i.e., the phenomenon of emission of light in response to the passage of a radiated particle through a material. As the particle travels through the scintillator, it deposits some of its energy, leading to the excitation of electrons within the scintillator. These electrons subsequently emit light as they return to their base energy states. The number of excited electrons is proportional to the energy deposited by the particle which, in turn, determines the number of emitted light photons. In this way, the scintillator responds to each detected particle with an impulse of light, whose intensity is proportional to the particle energy.

The scintillation light is then converted into a measurable electrical signal, proportional to the detected radiation. The most common component employed for this purpose is the photomultiplier, although photodiodes can also be used [4]. A graphical representation of a scintillator coupled to a photomultiplier is shown in Figure 1. Photo-Multiplier Tubes (PMTs) consist of a photocathode, a series of dynodes, and an anode. Incoming light photons from the scintillator hitting the photocathode cause electrons to be ejected from its surface by photoelectric effect. A high-voltage source, typically up to 2 kV, is used to accelerate the electrons through a focusing electrode. When striking a dynode at high speed, each electron causes multiple secondary electrons to be ejected, so that a cascade of electrons is created in the photomultiplier, amplifying the signal. The electrons are then collected on the anode, producing an
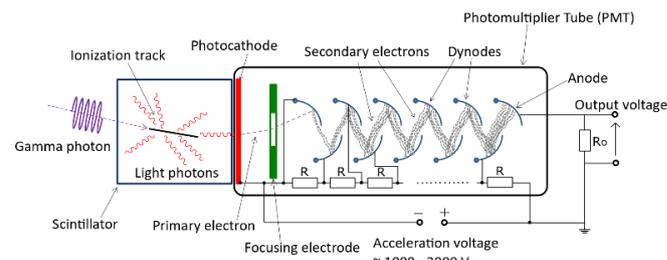

Figure 1. Representation of a scintillator coupled with a photomultiplier within a gamma spectroscopy system.

electrical current pulse. A transimpedance amplifier, or a resistor, is then used at the output to convert the current into voltage pulses, which can then be acquired by an ADC and digitally post-processed.

The shape of the voltage pulse corresponding to the incoming radiation is determined by the employed scintillator hardware and by the loading circuit of the photomultiplier. The general mathematical description for a voltage pulse at the anode of the photomultiplier after a single scintillation event is given by [4]:

$$V(t) = \frac{1}{\lambda - \theta} \frac{\lambda Q}{C} \left(e^{-\theta t} - e^{-\lambda t} \right), \qquad (1)$$

where λ is the decay constant of the scintillator, θ is the reciprocal of the time constant of the anode circuit, Q is the total charge collected over the pulse duration, and C is the combined capacitance of the anode and its loading circuit. The amplitude of the pulse is proportional to the charge collected at the photomultiplier anode, which is linearly dependent on the energy released by the particle during the scintillation event.

An example of voltage pulse shape captured from a scintillation detector is shown in Figure 2. Provided that λ and θ are system constants, the pulsed voltage waveform realises a fixed double-exponential shape. The frequency spectrum of such waveform fades out below the noise floor at around 70 MHz, which is then considered as the target bandwidth of the acquisition system, while any spurious frequency content above 70 MHz will be filtered out digitally. To estimate the maximum slew rate of the pulse, the acquired waveform is interpolated with a 9th-order polynomial, and then differentiated, as shown in Figure 2. The resulting maximum slew rate of the pulse is $SR_{MAX} =$76.5 V/µs.

Figure 3 shows the block diagram of the complete spectroscopy system under development at the NCBJ. In the expected final configuration, the voltage pulses from the photomultiplier will be acquired on a FPGA Mezzanine Card (FMC) connected to a Xilinx ZedBoard Zynq-7000 FPGA board. The FMC consists of an ADC, as well as of the circuitry for signal conditioning such as amplification, attenuation, inversion, or level shifting, to ensure the best compliance with ADC specifications (see Section 3). Moreover, the FMC contains the ADC clock, as well as the I2C protocol signals and power supply.
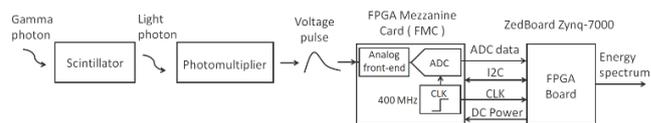

Figure 3. Block diagram of the spectroscopy system under development at the NCBJ.

Once the signal is sampled, the digital post-processing for obtaining the energy spectrum is carried out at high-speed by the FPGA. In particular, the post-processing aims at discriminating the individual pulses and obtaining a numerical value proportional to the energy. This can be achieved either by applying pulse integration or by considering the pulse peak. As mentioned in the Introduction, the values corresponding to a series of scintillation events are then distributed into bins of a histogram, creating the so-called energy spectrum. Eventually, the spectrum displays the number of measured counts (y-axis) for a set of energy channels (x-axis).

As an example, Figure 4 shows the energy spectrum for Cobalt-60, a standard material often used for the preliminary calibration of the spectroscopy system. In fact, Cobalt-60 is an isotope displaying two main peaks of the spectrum (C and D in Figure 4) at known precise energy levels (1.1732 MeV and 1.3325 MeV, respectively) representing the energy of gamma rays emitted during its radioactive decay [4]. In the calibration process, this information is then used to scale the energy channels on the x-axis in MeV. The other measured peaks (A and B in Figure 4) correspond to the phenomena of back-scattering and Compton scattering [4].

3. FRONT-END PROTOTYPE DESIGN

A stand-alone prototype ADC front-end board was designed for testing those components to be eventually mounted on the FMC card of the final spectroscopy system shown in Figure 3. The prototype board implements the ADC analogue front-end, the power supply circuitry, the I2C communication interface, and the clock generation to be used for the ADC as well as for the FPGA board. To allow for the linearity characterisation of the front-end alone, the prototype does not include the target ADC for the final application (ADS5474 monolithic pipeline ADC from Texas Instruments [20]), which features 14-bit resolution and sampling rate of 400 MSa/s. Such ADC is differential with a full-scale input of 1.1 V (single-ended) or 2.2 V (differential), requiring a common mode voltage of 3.1 V.

As previously discussed, the ADC analogue front-end should serve two main purposes. Firstly, it should perform attenuation and filtering. Indeed, to maximise the Signal-to-Noise Ratio
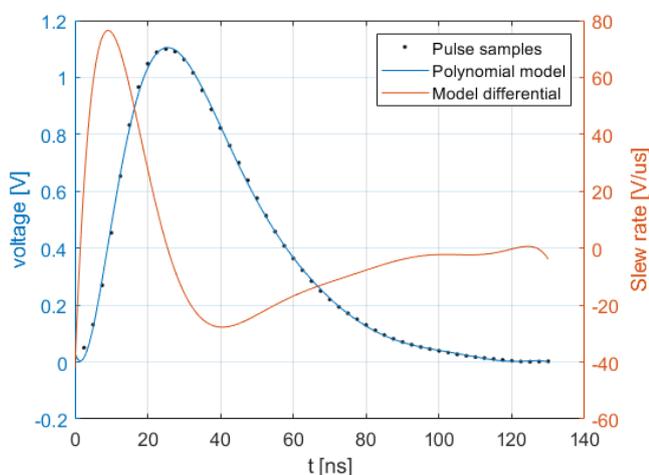

Figure 2. Oscilloscope acquisition of the response for a scintillation detector (black dots) used at NCBJ, polynomial interpolation (blue curve) and its time-differentiation for maximum slew-rate estimation (red).
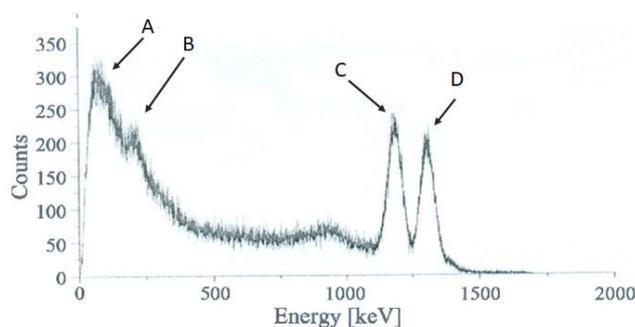

Figure 4. Example of an energy spectrum for Cobalt-60. Edited from [19].

(SNR) of the system, the range of amplitudes of the measured pulses from incoming radiation should correspond to the full-scale of the target ADC. While the voltage amplitudes at the output of the detector could be coarsely adjusted by changing the supply voltage of the photomultiplier, it is desirable to include, by the front-end, a software control functionality to digitally fine-tune the input voltage amplitude. In particular, as from the desired specifications, the gain resolution should be higher than 1 dB, while the digital control should be carried out through the I2C interface, readily available with a connector on the FMC.

Secondly, the front-end is supposed to protect the ADC by means of an analogue limiter circuit. Such ADC protection should clamp input voltage pulses of up to an order of magnitude above the ADC full-scale, providing sufficient protection from unwanted cosmic pulses which could damage the ADC. At the same time, clamping should be sufficiently fast, given that the pulse rise-time at the output of the scintillator is in the order of 10 ns. Moreover, a minimum of 70-MHz acquisition bandwidth is requested to completely capture the spectrum at the pulsed output of the detector.

3.1. Signal Conditioning Stage

The block diagram of the designed ADC front-end is shown in Figure 5. It is composed of a diode used for protecting the circuit from the ns-range over-voltage pulses, a digital step attenuator (DSA) for the adjustment of the measurement range, a fully differential amplifier (FDA) for signal buffering and single-ended to differential conversion, and an anti-aliasing filter.

The input parasitic capacitance (C_P) of the front-end should be sufficiently low to allow for the requested bandwidth $f_{BW}=70$ MHz. Considering an input resistance $R_{IN} = 50\ \Omega$, the parasitic capacitance must satisfy $C_P < \frac{1}{2\pi f_{BW}R_{IN}} \cong 45.5$ pF. In the proposed solution, a first clamping stage is embodied by a transient-voltage-suppression (TVS) diode from Nexperia (PESD5V0C1BSF), with a rated $C_P = 0.2$ pF and a reverse stand-off voltage of 5 V. The chosen TVS diode is bidirectional, meaning that it will protect against both positive and negative transients, as the pulse polarity depends on the configuration of the radiation detector.

To provide a flexible control across the overall gain of the signal conditioning chain, a digital step attenuator (DSA) was used. A 6-bit DSA from Analog Devices (HMC472A) with a variable attenuation from 0.5 dB to 31.5 dB in 0.5-dB steps was chosen for the design. The attenuation is set directly by TLL/CMOS-compatible input pins, which can be interfaced with I2C control.

Signal conversion from single-ended to differential is required to feed the ADC. Typical solutions include a balun or a Fully Differential Amplifier (FDA). While a balun would introduce less additive noise, an FDA can provide a suitable additional gain. Moreover, while the TVS diode can protect from the largest pulses, the pulse voltage amplitude must be adapted to the ±1.1 V full-scale range of the targeted ADC. In this sense, the FDA can provide the necessary additional clamping stage. Eventually, an FDA from Texas Instruments (LMH6553) was chosen, featuring voltage-controlled output clamping, 900-MHz bandwidth, and a slew rate of 2300 V/μs. A resistive network for the FDA was optimised by MATLAB and LT-Spice simulations to obtain an input impedance of 50 Ω and voltage gain of 2 V/V, allowing to compensate all insertion loss potentially arising in the system. A 10-pF capacitor was placed at the FDA output along
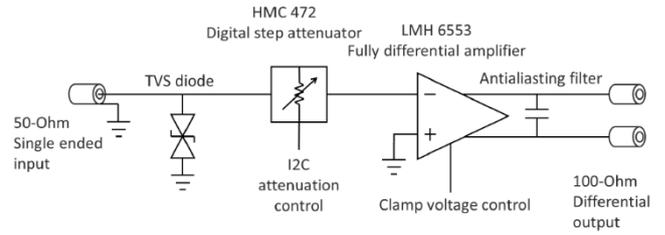

Figure 5. Block diagram of the designed ADC analogue front-end.

with two 50-Ω output matching resistors to implement an anti-aliasing RC filter with a cut-off frequency of ~ 160 MHz.

3.2. ADC reference clock

Beyond the signal conditioning, the designed prototype board is also aimed at testing a low-jitter 400-MHz clock for the ADC. In this context, let us consider the main noise sources impacting the total SNR of the ADC (SNR_{ADC}), which can be calculated as:

$$SNR_{ADC}(dB) = -20\log\sqrt{10^{-\left(\frac{SNR_Q}{20}\right)^2} + 10^{-\left(\frac{SNR_T}{20}\right)^2} + 10^{-\left(\frac{SNR_J}{20}\right)^2}}, \quad (2)$$

where SNR_Q (in dB) is due to quantisation noise, SNR_T (in dB) is due to thermal noise, and SNR_J (in dB) is due to total jitter. In high-speed pipelined ADCs such as the one considered here, the thermal noise limits the SNR at low input frequencies, while the clock jitter mainly influences the high frequencies [19].

The SNR_Q for a full-scale sine wave input can be expressed by the well-known formula $SNR_Q(dB) = (1.761 + 6.02\ N)$, N being the number of bits of the ADC. Considering that the nominal resolution of the ADS5457 is 14 bits, it holds that $SNR_Q = 86.04$ dB. As from datasheet [20], the limit due to thermal noise is estimated at $SNR_T = 70.3$ dB, while the estimated overall maximum performance is $SNR_{ADC} = 70.1$ dB. Using the data in the formula above, one can deduce a requirement for the noise due to jitter, resulting in $SNR_J \geq 75.2$ dB.

Let us consider the relationship between the total jitter affecting the sampling process and the resulting impact on the SNR [18]:

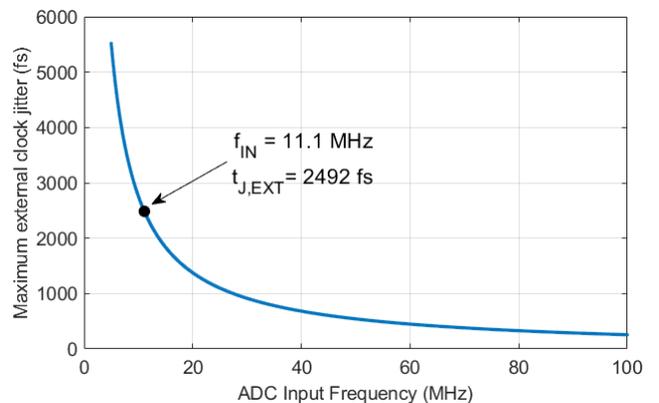$$SNR_J = -20\log\left(2\pi f_{IN}t_{J,TOT}\right), \quad (3)$$

Figure 6. External clock source RMS jitter ($t_{J,EXT}$) required to keep $SNR_{ADC} >$ 70.1 dB, as a function of the input frequency (f_{IN}).
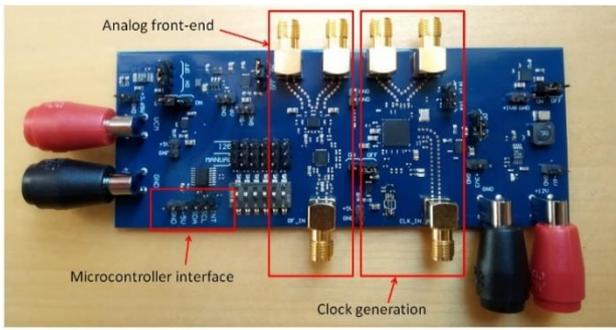
Figure 7. Photo of the designed front-end board.

Figure 9. Phase noise of the TI LMK03318 clock generator with the crystal oscillator reference (10 output correlations enabled). The plot includes the spurious components due to the power supply (in blue).

where f_{IN} is the frequency of the input signal to be sampled, and $t_{J,TOT}$ is the RMS value of the total jitter. The total jitter impacting on the A/D process is a function of the timing jitter of the external clock source ($t_{J,EXT}$) as well as the aperture jitter ($t_{J,IN}$) of the ADC, which is dependent on the noise of the internal clock buffer [20]:

$$t_{J,EXT} = \sqrt{t_{J,TOT}^2 - t_{J,IN}^2}, \tag{4}$$

where $t_{J,IN} = 103$ fs for the ADS5457. Figure 6 shows the relationship between the requirement for maximum RMS timing jitter of the external clock ($t_{J,EXT}$) and the input sinewave frequency (f_{IN}). Given that the maximum slew rate of the voltage pulses at the output of the photomultiplier is $SR_{MAX} = 76.5$ V/μs, and considering that this value corresponds to a pure sinewave of $f_{IN} = \frac{SR_{MAX}}{A2\pi} \cong 11.1$ MHz, the plot in Figure 6 indicates that it must hold $t_{J,EXT} \leq 2492$ fs to keep $SNR_J \geq 75.2$ dB $SNR_{ADC} \geq 70.1$ dB).

To satisfy the design jitter requirements, a clock-generating IC (LMK03318 from Texas Instruments) was combined with a 25-MHz crystal oscillator reference (TXC 7M-25MEEQ). Also, an additional input port provides the option of connecting an external reference. The IC is controllable by I2C interface and should deliver RMS timing jitter in the 100-fs-range as from datasheet, which is deemed enough to satisfy the minimum requirement for the SNR_{ADC}.

3.3. Board implementation

A four-layer Printed Circuit Board (PCB) was designed to implement the front-end prototype. The top layer is used for routing all analogue and a subset of digital traces, as well as for mounting all the components. The second layer is a ground plane, which serves as the reference plane for controlled-impedance traces on the top layer. The third layer is used for
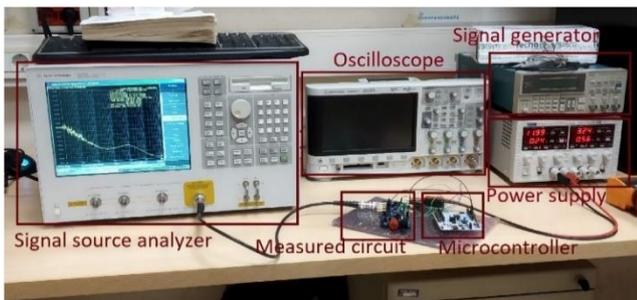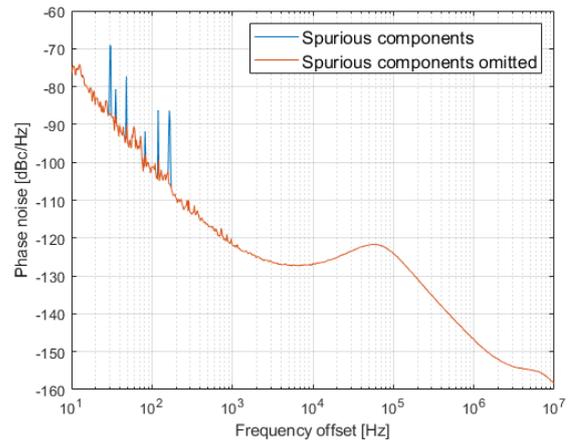

Figure 8. Set-up for the characterisation of the phase noise of the on-board clock of the ADC.

routing power connections, while the bottom layer contains the remaining digital traces. To preserve signal integrity, all signal traces in the analogue front-end, as well as the clock signal path, were calculated to have 50-Ω characteristic impedance. In addition, these traces were also shielded from interference via fences. Special care was also taken when laying out the step-down switching regulator, as it is likely to generate the most Electro-Magnetic Interference (EMI).

The board is equipped with gold-pin headers for I2C communication with an external device, e.g., a microcontroller. To control the DSA via the I2C interface, a MAX7320 I/O expander was used, and a set of headers allows to select the control of the DSA either by I2C or manual control by a Dual In-line Package (DIP) switch.

Concerning power supply, Linear Low-Dropout (LDO) regulators offering voltage stabilisation, very low noise, and no additional interferences affecting ADC readouts, are used to convert the 12 V supply received from the carrier board into lower voltages. However, LDOs are quite inefficient when the difference between regulated output voltage and input voltage is large. The lowest regulated voltage is 1.8 V, as required by the output buffers of the clock generator, causing the LDO to work at efficiency below 15%. To avoid excessive power dissipation in this specific case, the 12 V input voltage was first converted to 6 V with a high-efficiency step-down switching regulator (LT8069A from Analog Devices), offering efficiency above 90%. The switching frequency was set to 1.8 MHz to allow for a small inductor in the step-down converter, which is important on an FMC board with limited space. Additionally, the device has spread spectrum functionality, lowering EMI [21] and improving signal integrity. The output 6 V voltage is eventually converted into the required positive and negative supply voltages using LDOs. Two sets of gold-pin headers are also used for every linear regulator to enable the user to switch it on/off, and to test-point the regulated voltage. A photo of the manufactured board is shown in Figure 7.

4. EXPERIMENTAL CHARACTERISATION

In this Section, the characterisation performed for the designed prototype are described. They include phase noise measurement for the on-board ADC clock and a metrological characterisation in terms of Total Harmonic Distortion (THD)
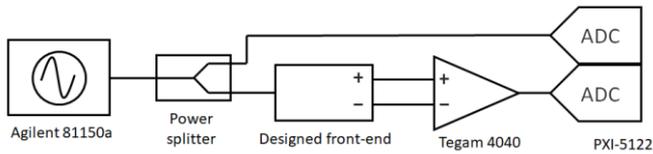
Figure 10. Block diagram of the measurement setup for the characterisation of the ADC analogue front-end.

and Effective Number of Bits (ENOB) for the whole acquisition path including the front-end. Also, the behaviour of the front-end is measured under application-like pulsed excitation.

4.1. Clock jitter characterisation

The clock-generating device (LMK03318) was programmed through I2C interface, connecting the circuit to a microcontroller board (Nucleo-F446RE). The device was configured to provide one differential output of a 400 MHz signal at the SMA port, while all other outputs were terminated with 100-Ω resistors. To evaluate the RMS time jitter, phase noise measurements were carried out by means of the setup in Figure 8 using the Agilent E5052A signal source analyser and a TTI CPX400DP power supply for powering the prototype board.

Phase noise measurements provide a single sideband noise density spectrum of a signal at different offset frequencies from the carrier at 400 MHz. The RMS jitter value is found by integrating the phase noise spectrum over a range of offset frequencies (in this case, 10 Hz - 10 MHz). For this device, the obtained RMS jitter is ≈ 440 fs in the configuration with on-board 25-MHz reference, despite the presence of spurious components coming from the power supply, e.g., at 30 Hz, 50 Hz, 120 Hz and 160 Hz (see Figure 9). When removing these most evident spurious components via software, the RMS jitter value reaches ≈ 312 fs. At the same time, it is worth noting that no spurious components are found at 1.8 MHz (corresponding to the switching frequency of the main on-board power converter), demonstrating that EMI was well contained. The measured jitter performance validates the suitability of the designed clock generation.

4.2. Metrological characterisation of the acquisition channel

A metrological characterisation of the prototype front-end alone, i.e., neglecting any effect of ADC at the output, was performed. To this aim, we adopt the measurement setup shown in Figure 10 and Figure 11. The Arbitrary Waveform Generator (AWG) output (Agilent 81150a) is split by means of a 50-Ω-terminated divider to feed, with the same excitation, two parallel acquisition paths. In the first path, the split signal is applied to the device-under-test (DUT), i.e., the analogue front-end. A
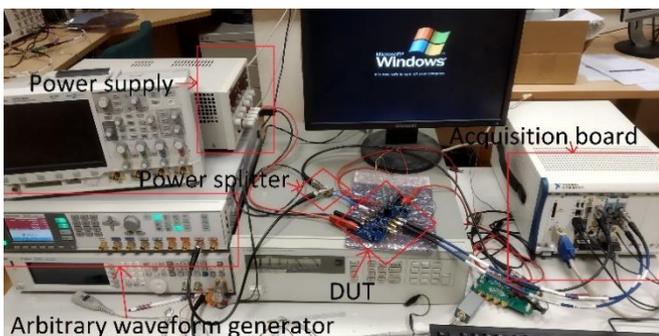
high-linearity instrumentation amplifier (Tegam 4040) was used to transform the differential output of the front-end into the first channel of a 100-MHz, 100-MSa/s, 14-bit digitiser board (National Instruments PXI-5122) which, given the much higher linearity and lower noise, is here considered as an ideal acquisition device. In the second path, i.e., the reference acquisition path, the output of the splitter directly feeds the second channel the PXI-5122 digitiser board.

A preliminary test procedure was carried out using sinusoidal tone excitations up to 1 MHz, so to avoid introducing any spurious effect due to the digitiser, e.g., the initial roll-off of the anti-alias filter. The measurement data was then processed according to Standard IEEE 1241 [22]. For this specific characterisation, no reference acquisition is needed, thus only the receiver chain comprising the front-end under test was used. The considered figures of merit (FoM), i.e., THD and ENOB, are reported in Figure 12 and Figure 13, respectively, for a set of acquired frequencies and amplitudes. As can be seen, the prototype front-end introduces a clear dependency on the input signal amplitude. While the distortion at -12 dBFS is negligible over the measured frequency range, it substantially deteriorates when the excitation approaches the full scale, reporting THD as high as -30 dB and minimum ENOB of around 5 at -1 dBFS. This could be attributed to the nonlinear characteristic of the TVS diode, as well as to the low-frequency performance of the switching circuitry inside of the digital step attenuator.
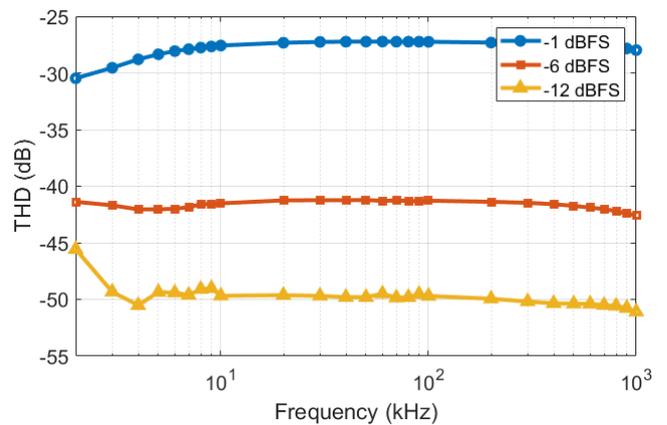

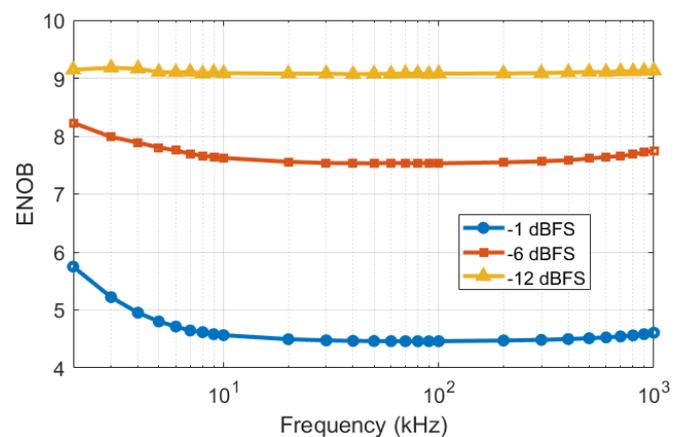Figure 12. Total harmonic distortion (9 harmonics) of the acquisition chain including the ADC front-end.

Figure 13. Effective number of bits of the acquisition chain including the ADC front-end.

Figure 11. Picture of the measurement setup for the characterisation of the ADC analogue front-end.

4.3. Application-like pulse measurements

The prototype front-end was tested for application-like spectroscopy measurements. Indeed, as discussed in Section 2, in a realistic scenario the front-end would only receive specific signals, namely exponential pulses of a given duration and different amplitudes. Therefore, an additional characterisation was performed employing pulsed excitations modelled from experimental data of an actual scintillator. These pulsed waveforms could be easily generated by programming the AWG yet within its 50-MHz limit in high-amplitude mode. Then, the impact of the front-end on the pulse shape was quantified by comparing the waveforms distorted by the front-end under test with those acquired through the ideal reference path.

Considering that the PXI-5122 is not as fast as the ADS5474 ADC targeted for the final application, slower pulses excitations with 1-μs and 0.5-μs pulse widths were used to allow for a sufficiently high number of acquired samples per pulse, yet respecting the pulse shape produced by the detector. Both positive and negative polarities were considered, and sequences of 20 pulses with increasing amplitudes from zero up to the full scale of the ADC front-end were programmed into the AWG. All acquired signals were normalised in amplitude and delay to allow for numerical comparison. Additionally, spectrum equalisation was performed to compensate for the baseline wander effect due to the presence of AC-coupling capacitors in the front-end.
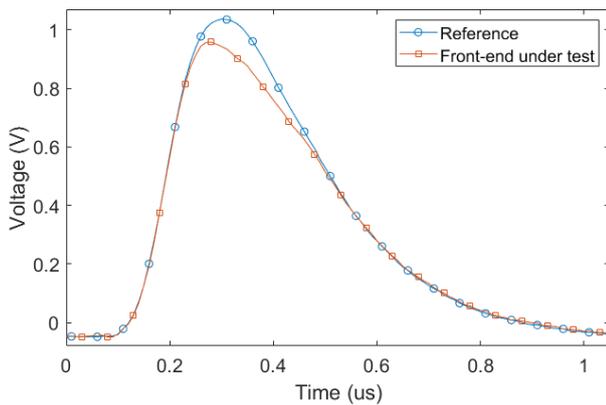
To characterise the performance of the front-end with respect to the ideal reference, two quantities were used. Firstly, the Normalised Root Mean Square Deviation (NRMSD) between the waveforms acquired from the two channels was calculated. Secondly, each of the pulses was integrated, as done for gamma spectroscopy measurements. Then, the NRMSD between the integral values calculated from the actual and reference receivers were obtained, quantifying the deviation that would directly map into the energy spectrum of the measured material. Tables 2 and 3 report the calculated deviations, while Figure 14 and Figure 15 show the shape of a single pulse at full scale amplitude for both acquisition paths. While the negative pulses do not show substantial deviation from the reference, the positive pulses are significantly distorted, hinting at the presence of nonlinear dynamic effects by the front-end.

5. DIGITAL LINEARISATION

To improve the linearity performance of the front-end under test, a DPD (i.e., digital linearisation) method was implemented. With post-distortion, the acquired signals are post-processed exploiting an inverse modelling of the whole receiver path. To this aim, we used a memory polynomial model, a well-known and effective formulation derived from the Volterra series representation, where the memory cross-terms are neglected [13]. Such a mathematical description is well suited for modelling

Figure 14. 1-μs positive pulse with full-scale amplitude, after passing through the two signal acquisition chains (reference and the one including the DUT).

Figure 16. Total harmonic distortion (9 harmonics) of the acquisition chain including the ADC front-end after digital post-distortion, measured at -1 dBFS.

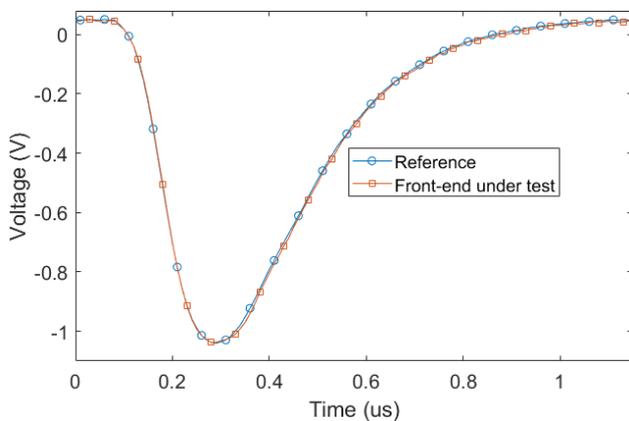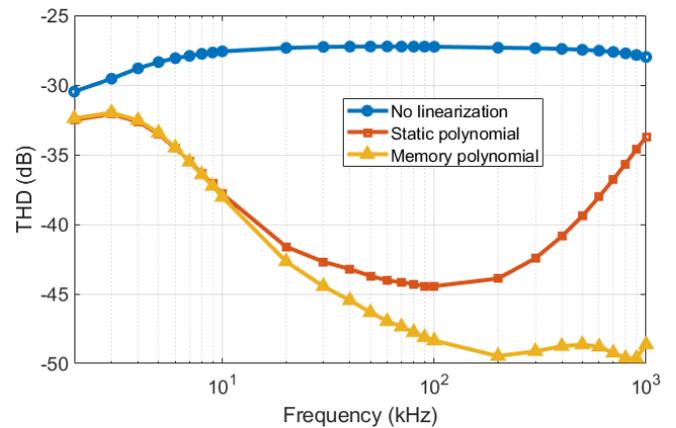
Figure 15. 1-μs negative pulse with full-scale amplitude, after passing through the two signal acquisition chains (reference and the one including the DUT).
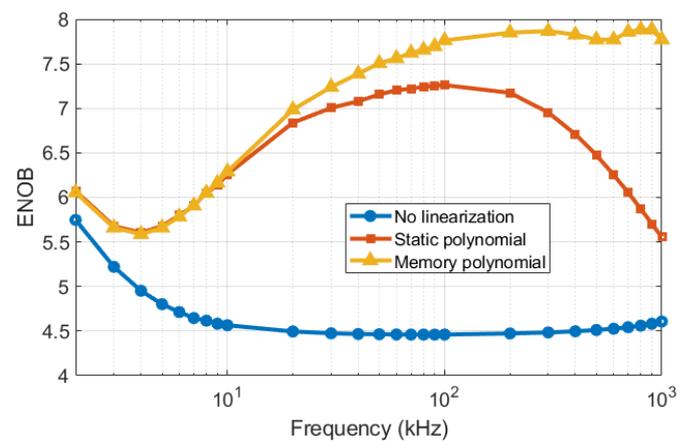

Figure 17. Effective number of bits of the acquisition chain including the ADC front-end after digital post-distortion, measured at -1 dBFS.

the nonlinear dynamic behaviour, and it finds broad use in digital pre-distortion of radiofrequency (RF) power amplifiers. The memory polynomial model is formulated as follows [13]:

$$y(n) = \sum_{m=0}^{M} \sum_{k=1}^{K} a_{mk} x(n-m) |x(n-m)|^{k-1}, \qquad (5)$$

M being the memory depth and K the nonlinear order. In theory, a high model order could provide high prediction accuracy, as it would better describe stronger nonlinearities. However, the identification of many model coefficients can often become ill-conditioned, since increasingly larger dataset of independent measured responses is needed to properly fit all coefficients. In this research, tests were carried out by progressively increasing K and M for a dataset of application-like pulsed waveforms; it was found that increasing the model order beyond $K = 5$ and $M = 3$ did not provide improved prediction capabilities. Out of the different tests, two cases were considered: a static ($M = 0$) polynomial model with $K = 5$, and a memory polynomial model with $K = 5$ and $M = 3$.

Rather than inverting the direct model by means of iterative or nonlinear optimisation algorithms, an indirect coefficient learning approach was used for the identification of the inverse model from time-domain measurement data, using the method in [23]. In a first characterisation, the inverse model was trained on a global dataset composed by acquisitions of sine-wave excitations at 10 kHz, 100 kHz, and 1 MHz. Then, a new experimental characterisation (again, according to IEEE 1241-2010) of the whole receiver chain composed by the combination of the analogue front-end and the DPD was performed and repeated by sweeping the input frequency from 1 kHz to 1 MHz. The THD and ENOB for the linearised receiver are plotted in Figure 16 and Figure 17, respectively. In the 1 kHz-1 MHz range, an improvement in THD of up to 15 dB was obtained with the static polynomial model, and of up to 20 dB with a memory polynomial model. The corresponding improvement in ENOB is more than 2 bits using the static polynomial model, and more than 3 bits using the memory polynomial model. It can be noticed that the linearisation is particularly effective in the band from 10 kHz to 1 MHz, which corresponds to those particular frequencies used for post-distorter coefficient training.

DPD was also applied for the acquisition of pulsed waveforms. In this case, the inverse models were separately trained for 0.5-µs and 1-µs pulse lengths, as well as for positive
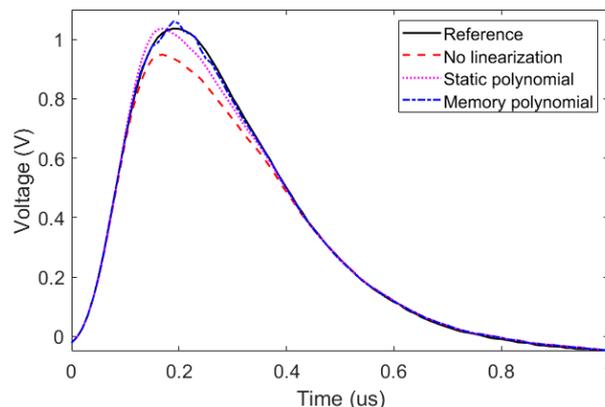

Figure 18. 1-µs positive pulse with full-scale amplitude after digital post-distortion.

and negative polarities. Figure 18 shows the pulse shape obtained after post-distortion using different models, and in comparison, to the reference channel. Table 1 and Table 2 summarise the values of the deviations from the reference in all tested cases. A significant reduction in the deviations was achieved for positive pulses, which showed the highest distortion. For example, the NRMSD was lowered more than four times in the case of 1-µs pulses. For negative pulses, the post-distortion had less impact, as the behaviour of the front-end was found to introduce less distortion. Using an inverse model with memory brings a further improvement only in the case of 1-µs positive pulses, as the other cases do not show substantial dynamic effects.

6. MEASUREMENTS USING THE SPECTROMETRY SYSTEM

The proposed methodology was tested with the complete spectrometry system setup at the NCBJ, corresponding to the block diagram previously introduced in Figure 3. The photo of the deployed system is shown in Figure 19. It includes an in-house Lanthanum Chloride scintillator developed at the NCBJ, coupled to the PMT and placed next to a source of gamma radiation, namely a sample of Caesium-137 (behind the green lead shield). The PMT is supplied with 1.6 kV from a high-voltage source. The FMC board includes the already introduced ADS5474 dual-channel ADC, while a Xilinx ZC-702 FPGA carrier board contains the Zynq-7000 SoC for real-time digital processing of the sampled data.

The voltage signal from the radiation detector is divided via a resistive power splitter into reference and test paths, following the same approach as in Figure 10 and Figure 11 for the PXI-based test setup previously adopted. The reference path is

Table 1. NRMSD (%) with and without MP-based post-distortion for different pulsed excitations.

Post-distortion	Positive pulse polarity		Negative pulse polarity	
	1 µs	0.5 µs	1 µs	0.5 µs
None	5.19	3.34	1.31	1.77
$K = 5, M = 0$	2.39	1.71	1.23	1.75
$K = 5, M = 3$	1.2	1.09	1.0	0.83

Table 2. Integral NRMSD (%) with and without MP-based post-distortion for different pulsed excitations.

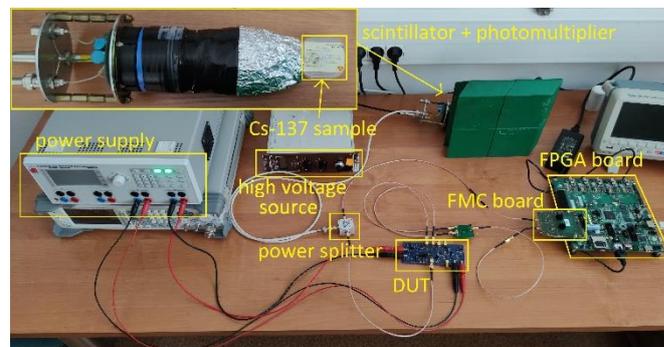| Post-distortion	Positive pulse polarity		Negative pulse polarity	
	1 µs	0.5 µs	1 µs	0.5 µs
None	3.44	2.62	1.14	0.88
$K = 5, M = 0$	1.35	1.19	1.03	0.84
$K = 5, M = 3$	0.97	1.0	1.03	0.79

Figure 19. The gamma spectroscopy measurement set-up at NCBJ, including the source or radiation (Caesium-137), the analogue front-end (DUT) and the two-channel acquisition system.

Table 3. NRMSD (%) and integral NRMSD (%) w/ and w/o MP-based post-distortion for the pulse waveform measured with the NCBJ acquisition system in Figure 19, using Caesium-137 as a radiation source.

Post-distortion	NMRSD (%)	Integral NMRSD (%)
None	5.86	5.52
$K = 5, M = 0$	3.8	1.99
$K = 5, M = 3$	1.98	1.09

directly connected to one of the digitiser channels, while the test path consists of the designed analogue front-end board, i.e., the Device Under Test (DUT), whose output is connected to the second channel of the digitiser. The DUT is supplied from a HAMEG HMP4040 power supply.

The spectrometry setup was used to capture a dataset consisting of 10^4 events from the scintillator, whose associated voltage pulses are concurrently acquired by both the reference and test ADC channels. The pulses have a duration of ~100 ns and amplitudes of up to 1 V. The waveform of a single captured pulse is shown in Figure 20. Digital linearisation was applied to the captured pulses using the same approach as in Section 5. More precisely, the acquisitions from both reference and DUT paths allowed to identify the inverse DUT model, then to perform digital linearisation by adopting the same post-distortion model formulation and orders as in Section 5. As shown in Figure 20, the nonlinear pulse waveform displays a sensibly lower amplitude w.r.t. to the reference acquisition, as well as a distorted shape, whereas both the static and the nonlinear dynamic post-distortion allow for a linearised pulse acquisition.

Just as performed in Section 5, the individual pulses were integrated to calculate a value directly proportional to their energy. Also, in this case, the deviation between the channels is quantified using NRMSD between the waveforms as well as NRMSD between the integral values computed from the waveforms. The obtained values confirm that the deviation from reference is significantly reduced by the digital linearisation. In particular, the static polynomial model ($K = 5$, $M = 0$) reduced the NRMSD from 5.86% to 3.8%, while adding the memory terms ($K = 5$, $M = 3$) allowed a further reduction down to 1.98%. Similarly, the NRMSD of the integral values was reduced from 5.52% to 1.99% with the static polynomial model, and to 1.09% using the model with memory (see Table 3).

Finally, the energy spectrum from a 250-channel histogram of the integral values was estimated both with and without digital linearisation (Figure 21). As the pulses with low amplitude are
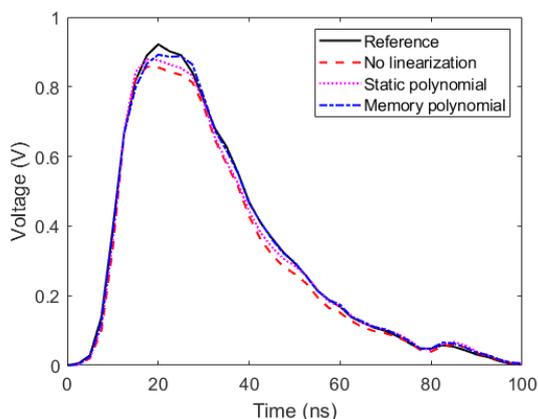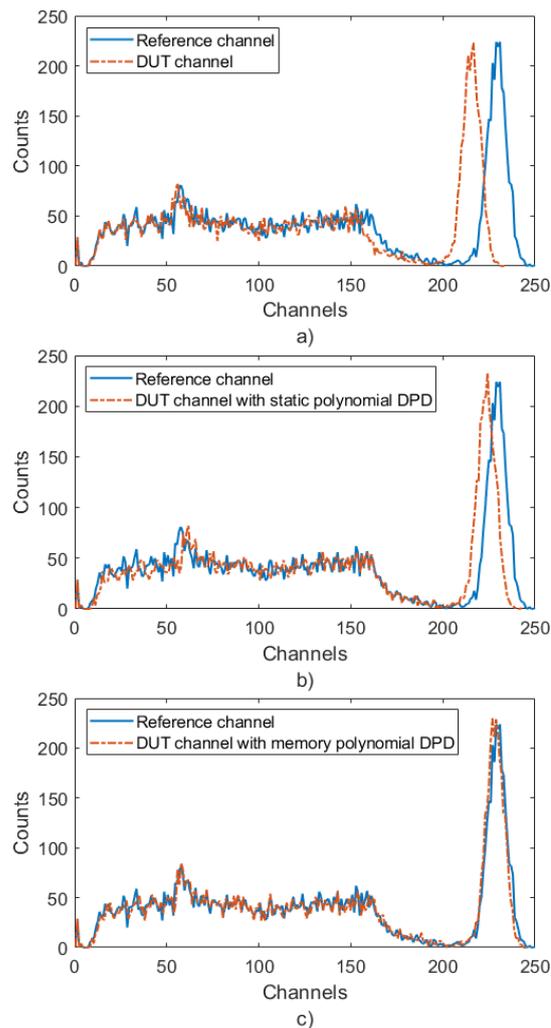

Figure 21. Energy spectrum of Caesium-137 estimated using the spectrometry setup including the designed analogue front-end a) without linearisation; b) with static DPD (MP model with $K = 5$, $M = 0$); c) with nonlinear-dynamic DPD (MP model with $K = 5$, $M = 3$). Full-scale energy is 723 keV.

less distorted, the lower energy part of the spectrum is reasonably similar to the reference. However, at higher pulse amplitudes (i.e., at higher energies) the whole spectrum content, and most notably the gamma photo-peak (~ 662 keV for Caesium-137), is shifted towards lower energies by non-compensated nonlinearities (Figure 21a). The energy spectrum linearised using the static model (Figure 21b) shows a reduced yet still substantial deviation, whereas the DPD with memory (Figure 21c) ensures the best alignment with the reference spectrum over the entire energy range.

7. CONCLUSION

In this work, the design, characterisation, and performance assessment of an analogue front-end for use in the gamma spectrometry system of the NCBJ was presented. The front-end was designed to properly condition the pulsed signals at the output of the detector and protect the receiver from high-voltage spikes due to cosmic radiation. It also provides a suitable, low-timing jitter clock reference for the ADC within the receiver.

An extensive characterisation of the protected receiver equipped with the designed front-end allowed to quantify the

Figure 20. Example of a pulse waveform from the radiation detector w/ and w/o digital linearisation. Comparison with the reference A/D acquisition.

reduction of the dynamic range inevitably caused by the analogue limiting stage, as well as by the necessary signal conditioning. A digital linearisation approach based on the identification of an inverse nonlinear dynamic model of the receiver, and its application for post-distortion, allowed to recover the necessary linearity to guarantee the accurate acquisition of the fast pulses generated by the radiation detector.

In-field experiments involving actual spectrometry measurements of a Caesium-137 radiation source confirmed the suitability of the designed front-end, as well as the effectiveness of the digital linearisation approach, which allows to compensate for critical peak shifts in the estimated energy spectra caused by receiver nonlinear distortion.

ACKNOWLEDGEMENT

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