



Multi-platform solution for data acquisition

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ABSTRACT

Analogue data acquisition is a common task which has application in several fields such as scientific research, industry, food production, safety, and environmental monitoring. It can be carried out either using systems designed ad-hoc for a specific application or by using general-purpose Digital Acquisition Boards (DAQ). Several DAQ solutions are nowadays available on the market, however, most of them are extremely expensive and come as commercial closed products, a factor which prevents users to adapt the system to their specific applications and limits the product compatibility to few operating systems or platforms. This paper describes the design and the preliminary metrological characterisation of a digital data acquisition solution based on the Teensyduino Development Board. The aim of the project is to create a hardware and software infrastructure suitable to be employed on several operating systems and that can be freely modified by the users when required. Teensyduino board is a well-known development platform which is characterised by high computing performance and USB support. Taking advantage of the Teensyduino features, the proposed system is easy to be calibrated and used, and it provides functions and performance comparable to many commercial DAQs, but at a significantly lower cost.

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1. INTRODUCTION

Several applications both in the research and industry fields require the digital acquisition of analogue signals and the subsequent signal processing. This task can be successfully carried out by employing Data Acquisition Boards, usually referred to as DAQ boards. These systems are typically able to acquire digital and analogue signals sending data to a host computer via USB port, for storage and further processing, and are widely employed in many applications, from imaging processing to acquisition of physical and chemical quantities, [1]-[3]. Many companies and universities daily use such general-purpose acquisition boards when it is not economically advantageous to develop a dedicated acquisition system.

As a matter of fact, the use of DAQ boards requires an easy interfacing with the host computer in order to carry out several operations including: board calibration [4] and configuration, data acquisition from several sources, and data saving. Typically, users are supported in such operations by a control and acquisition software, provided by the board manufacturer, which is installed on the host computer. Unfortunately, such software is in most of the cases compatible only with Windows OS [5].

Moreover, the software is usually provided as commercial closed-license application which cannot be freely modified or updated, so that users are dependent on the board manufacturer for firmware and software updates and for platform support. This factor is extremely important because it prevents the employment of the commercial DAQ in several applications where, due to other constraints, the use of Windows-based computers is not possible.

Few open-source solutions are available [6]-[8], but usually they lack in performance (especially in terms of accuracy) when compared with commercial DAQs. Other DAQs, instead, are developed for very specific applications [9] or they feature FPGA/DSP-based data processing which increases costs [10].

This work tries to tackle this issue, by providing a simple, thought powerful solution suitable for Data Acquisition regardless of the employed operating system. The proposed system is based on a Teensy board [11], easily available off-the-shelf and able to connect to host PCs via a serial 'emulated' USB. The USB port is also used to power both the Teensy and all the auxiliary circuits, therefore, no external power supply is required. Even though it is not possible to guarantee its compatibility for all future operating systems, the probability of a dropping

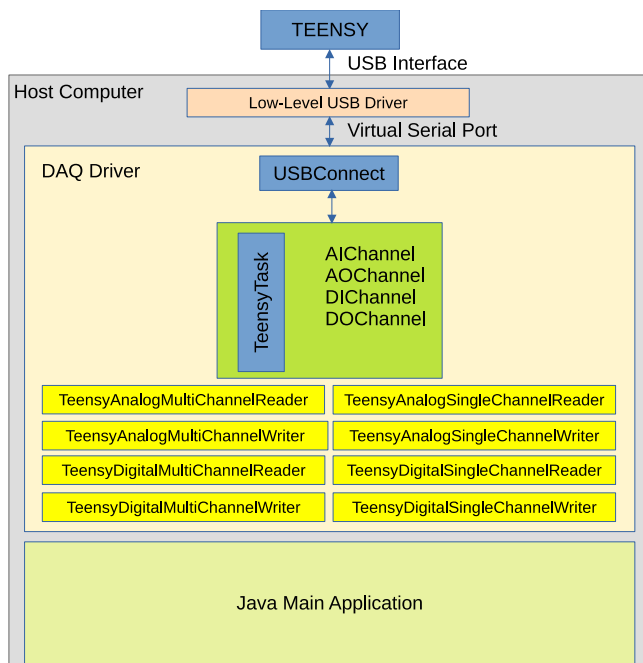


Figure 1. The developed software infrastructure which allows the board to be interfaced to a wide range of different platforms, including Windows, Linux and MacOS.

support is minimal due to the use of basic drivers, typically available for all machines.

The acquisition system is compact, easy to use and to calibrate. In particular, calibration is carried out either in-house, if a suitable DMM is available, or in a calibration laboratory. The DAQ provides also analogue and digital outputs which can be used to generate analogue signals and to interface with other systems. All these features are typically available only on extremely expensive commercial DAQs.

Two different solutions have been developed, either with or without external ADCs and DACs. The former, based on high-performing ADCs and DACs, can be extremely accurate and can provide outstanding performance, while the latter, based on the internal Teensy peripherals, has limited performance, but it has a really low cost. In this work both solutions are explored and, in both cases, suitable control software is provided so that the board use is simple and straightforward.

2. SOFTWARE INFRASTRUCTURE

In order to have a simple and ready-to-use acquisition system, the board should be able to work on almost any type of platform. This implies the development of a software infrastructure which is compatible with most of the machines and operating systems nowadays available on the market. To address this issue, the chosen solution was to rely on a layered software infrastructure, as shown in Figure 1. Java has been used for developing the software due to its high compatibility and portability on a very wide range of platforms, including Windows, Linux, and MacOS.

The Teensy board comes with a native USB Interface which embeds an 'emulated' serial port supporting data transfer rates similar the USB 2.0 Full-Speed Specifications. When the Teensy is connected to the host computer, it is recognized as a 'Virtual Serial Port' if a suitable low-level driver is installed. Such type of driver is available virtually for all operative systems/platforms and, in most cases, it is natively installed. The proposed solution makes use of the Fazecast multi-platform serial driver [12], but

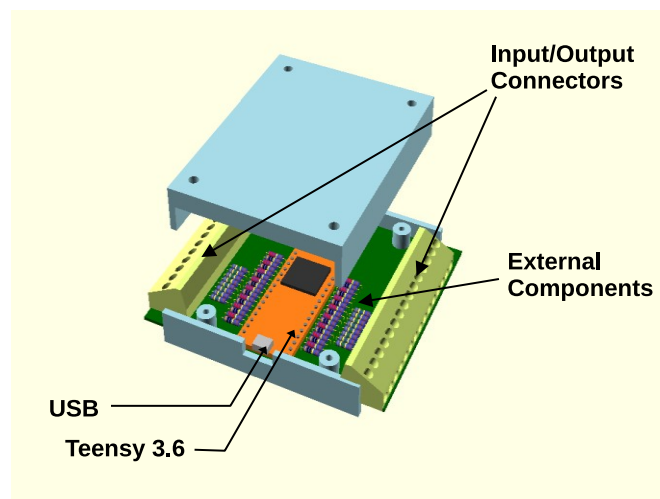


Figure 2. Structure of the ultra-low-cost Teensy-based DAQ Board. Inside the 3D-printed box, there is the Teensy 3.6, few passive components and the input/output connectors.

several other Java serial drivers could be used as well. The next layer is the DAQ Driver, which embeds all the control and data exchange tasks between the virtual serial port and the main application.

In particular, the DAQ Driver is based on a Java class named *TeensyTask* and all serial data interchange with the Teensy Board is confined inside another class called *USBConnect*. Any user wishing to employ the *DAQ Driver* simply has to instantiate a *TeensyTask* and add the required channels, either analogue or digital, input or output, using the method *CreateChannel* provided by one of the channels (*AIChannel*, ...). The user can set all the timing details by using the method *Timing*. Eventually, the user can instantiate one of the reader/writer methods (*AnalogSingleChannelReader*, ...) and decide the number of samples to be read and/or written. Finally, the main application provides a Graphical User Interface (GUI), which allows the users to configure all the DAQ parameters, visualize the acquired data and export them in several formats. If such application does not satisfy the requirements of a specific acquisition task, users can freely develop their own software taking advantage from the DAQ Driver. An alternative software architecture using Python is currently under development with the aim to further extend the range of platforms supported by the proposed DAQ solution.

3. TEENYDAQ BOARD WITHOUT EXTERNAL ADC

As a first case study, the Author developed an ultra-low-cost DAQ board using only a Teensy 3.6 Board and few passive external components, as it is shown in Figure 2. The board can be proposed for possible applications in different fields, such as the development of generic acquisition of analogue signals, impedance measurements, environmental and structural monitoring, corrosion protection also in the cultural heritage field, motor control for movable equipment and biomedical applications [13]-[16].

The board has a cost in the order of 30 \$ and it has dimensions and performance similar to the USB6001, a commercial DAQ deployed by National Instruments [17]. The DAQ is fully compliant with the software described in Section II.

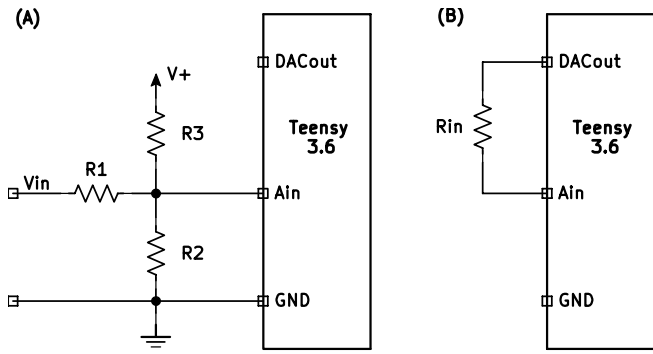


Figure 3. (A) Input passive conditioning network which allows the Teensy to measure bipolar signals in a fixed input range. (B) Simple configuration to test the ADC noise and accuracy performance for different input resistances.

3.1. Board Architecture

Teensy 3.6 contains a micro-controller with two Analog-to-Digital converters and two Digital-to-Analogue converters, plus several digital input/output pins. Therefore, it is possible to arrange a complete solution based only on this development board, adding only few passive components. Some possible configurations have been proposed in literature [18]-[19], however, some problems still exist:

- The ADCs can sample up to the speed of 1 MSPS, but the inputs are constrained to only positive voltages in the range from 0 V to 3.3 V. Usually, DAQ boards have bipolar input ranges which extend up to 10 V. It is possible to obtain bipolar ranges only with passive components, but at the cost of a reduced input impedance and accuracy.
- Commercial DAQs are able to measure very low-amplitude signals thanks to internal active amplifiers, but this cannot be achieved with passive component.
- The ADCs have a maximum nominal number of bits equal to 16, but the uncertainty and the noise limit the effective bit number to about 12. In addition, a low input impedance is required to maintain the 12-bit accuracy, so this limits the type of sources which can be used with the DAQ.
- The DACs are quite limited, as well. Despite their high sample rate capability, again the output voltage range is limited from 0 V up to 3.3 V, while commercial boards usually have bipolar outputs in the range of +/- 10 V.
- Digital input/outputs are limited to a maximum of 3.3 V and applying the usual TTL voltage of 5 V can damage the board.

The discussed limitations can be partially overcome. Figure 3(A) shows a possible solution for the unipolar Teensy ADC inputs. Basically, this is achieved by adding a fixed offset so that the Ain voltage is at the ADC range centre when the input voltage V_{in} is zero.

The relation between the ADC input voltage Ain and the input voltage V_{in} can be written as:

$$A_{in} = K + \alpha V_{in}, \quad (1)$$

where α is the attenuation factor of the input voltage and K is a fixed DC offset which is added to the scaled input voltage:

$$K = \frac{V^+ R_1 R_2}{(R_1 R_2 + R_1 R_3 + R_2 R_3)} \quad (2)$$

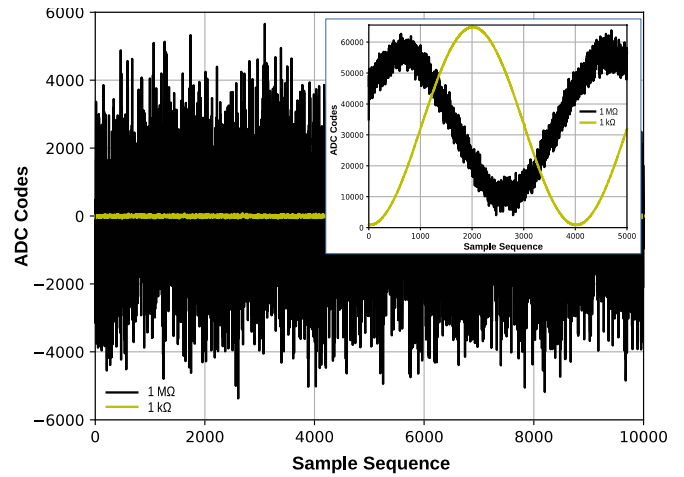


Figure 4. Example of DC voltage acquired with two different input resistances, respectively, of 1 k Ω to 1 M Ω . The inset shows the signal acquired in the same conditions when the DAC is programmed to output sine signal.

$$\alpha = \frac{R_2 R_3}{(R_1 R_2 + R_1 R_3 + R_2 R_3)} \quad (3)$$

By using this configuration, virtually any bipolar input voltage range can be obtained while keeping the ADC input within the allowed range by selecting the resistors R_1 , R_2 , and R_3 to satisfy the following equations:

$$K = \frac{R_{21}}{R_3 + R_{21}} \cdot V^+ = \frac{V_{ref}}{2}, \quad R_{ij} = \frac{R_i \cdot R_j}{R_i + R_j} \quad (4)$$

$$\alpha = \frac{V_{ref}}{2 V_{inmax}}, \quad (5)$$

where V_{ref} is the Teensy ADC reference voltage, usually equal to either 1.2 V or 3.3 V, and V_{inmax} is the maximum input voltage.

The equivalent input impedance can be easily calculated as:

$$R_{in} = R_1 + R_{23}. \quad (6)$$

As an example, by using $V^+ = V_{ref} = 3.3$ V and selecting resistors of $R_1 = 849$ k Ω , $R_2 = 300$ k Ω and $R_3 = 221$ k Ω , a maximum input of about 10 V and an input impedance of about 1 M Ω can be obtained without using any active component and selecting the resistors only from the E96, 1% series.

However, still some problems are present:

- The input impedance is quite high, in the order of 1 M Ω , but still lower than commercial DAQs whose typical input impedance is of the order of 1 G Ω . Moreover, a voltage appears on the input pins. In principle, this is not a problem, but it could either harm some circuits or interfere with their operation.
- The equivalent impedance at Ain pins is of the order of 115 k Ω while the Teensy specifications state that the analogue input impedance should be kept at the minimum possible value. While this might not be a problem, there are cases where the ADC accuracy cannot be guaranteed. This problem could be easily solved by inserting a buffer amplifier, but this would increase the cost and prevent a really simple system to be arranged.

- Using the same value for V^+ and V_{ref} makes the contribution of the V^+ uncertainty negligible, but the resistor uncertainty of 1 % may lead to an uncertainty on each input range of the order of 2 %. This means that in the absence of other corrections, at full input range a 2 % uncertainty should be expected (200 mV on the input value).

If such measurement uncertainty is not acceptable, there is a simple way of calibrating the system. As the scaling gain for each input may be slightly different, each channel must be individually calibrated. The solution is the use of a known voltage to be measured by each channel. As an example, by employing the Texas Instruments *LM4030AMF-2.5* voltage reference featuring an output voltage of 2.5 V with a 0.05 % maximum uncertainty and a temperature coefficient of 10 ppm/°C, the calibration can be easily performed for each channel.

The Author decided to put the *LM4030AMF-2.5* on the PCB and to take its output out on one connector pin without adding any digital switch for the calibration with the aim of maintaining the system cost as low as possible. In this way the calibration has to be done by manually shorting each input to the ground to measure K and then connect it to the reference output for measuring α . The values are then stored on the Teensy memory for automatically correcting the acquired data.

All these operations do not eliminate the problem related to the impedance on the input analogue pins on the Teensy. Under the best conditions, i.e., with hardware averaging enabled, differential mode and ADC clock slow enough, the accuracy is better than 13 bits, but if all these conditions are not met, the accuracy may severely degrade, especially if the impedance seen by the analogue inputs is high.

In order to test such performance deterioration, the configuration shown in Figure 3(B) can be used.

Using a DAC output lets users to change the signal amplitude so that it is possible to stimulate the Teensy ADC with a voltage which is inside the allowed range, while it is possible to observe the degradation of the sampled output signal by changing the input resistance R_{in} .

As an example, Figure 4 superposed two acquisitions carried out with a R_{in} of 1 k Ω and 1 M Ω . The difference in terms of noise performance is clear. Moreover, no change was observed by driving the DAC with different DC values. The inset shows, instead, the acquired data when the DAC is programmed to output a sine signal with the same two input resistances. The signals have a different phase as no phase adjustment was performed and have different amplitudes since the ADC loading effect is not negligible when using a resistance of 1 M Ω . In any case, the noise effect on the acquired signal is similar as in the case of DC values.

Computing the equivalent bits of the acquisition is not straightforward, as it depends on the acquisition purpose. In the worst-case scenario, i.e., if the instantaneous value of the signal is required, the equivalent bits can be obtained as:

$$Eq_{bits} = \log_2 \left(\frac{2^{16}}{\Delta} \right), \quad (7)$$

where Δ is the maximum difference between the real value and the measured value. The Author tested the ADC for resistances in the range from 1 k Ω to 1 M Ω by using two different ADC configurations:

- maximum sampling rate (about 200 kHz) and no hardware averaging;

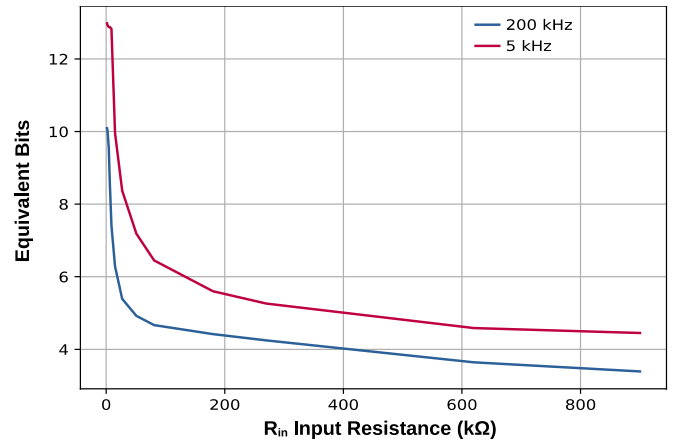


Figure 5. Equivalent bit number as function of the input resistance R_{in} . The two traces refer to the ADC acquiring in single ended mode with a sampling rate of 200 kHz (no hardware averaging) and 5 kHz (with hardware averaging of 32), respectively.

- slow sampling rate (about 5 kHz) and a hardware averaging of 32.

The results are shown in Figure 5, where the equivalent bit number is calculated as function of the input resistance. The figure shows how in the case of maximum speed the equivalent bits exceed 10 bits only when the resistance is negligible and severely degrades as the input resistance increases, while the equivalent bits are close to 13 when the speed is limited to 5 kHz. It is worth to note that this is the worst case and if, as an example, a sine signal is used and a sine amplitude is required, much better values can be obtained as the noise tends to spread over a wide frequency range. This is confirmed by the FFT of the acquired data. Figure 6, as an example, shows the Fourier Transform of the data acquired at a sampling rate of 100 kHz with an input resistance of 1 M Ω .

Apart from the peak at 50 Hz, which is expected when the source impedance is high and no shielding is done, it is clear how the noise spread on a large frequency range.

3.2. Performance

The DAQ which uses only the Teensy 3.6 and few external components has several advantages, including an extremely low

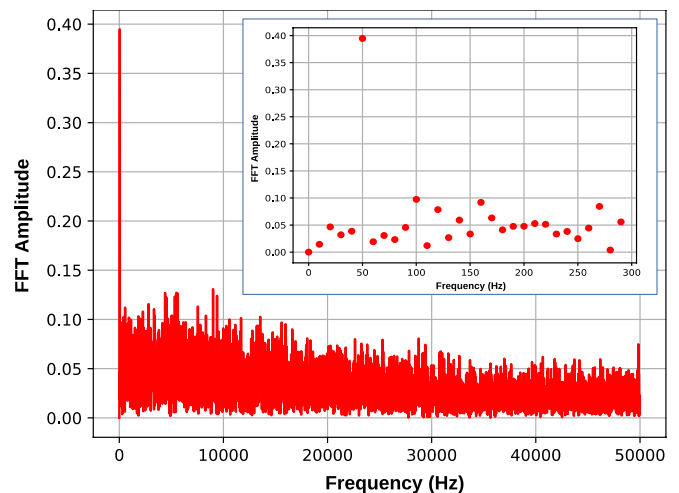


Figure 6. FFT of the acquired data in the case of a sampling rate of 100 kHz and an input impedance of 1 M Ω . The inset shows that the peak highlighted by the FFT is due to the 50 Hz mains noise which couples to the input when source impedance is high.

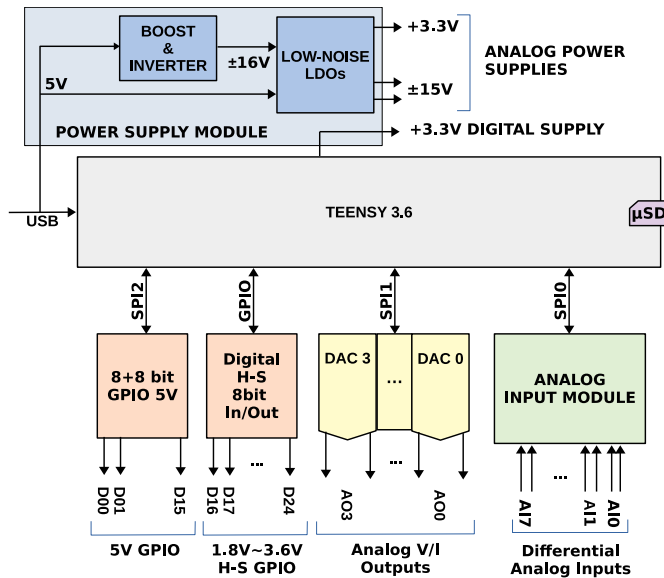


Figure 7. Block diagram of the high-performance DAQ board which employs the Teensy 3.6 and external ADC and DACs.

cost and a very compact size. Unfortunately, the absence of any active component at the input stages involves also several issues which can be addressed only partially. The lack of any gain stage at the input limits the capability of the DAQ to acquire signals with very low amplitudes. The relatively low input impedance limits the employment of the board to only low-impedance sources. Moreover, as shown by Figure 5, also at low input resistance (few $k\Omega$) there is an unacceptable signal degradation. Better results can be obtained when the Teensy 3.6 ADC is used with the hardware average and at a low sampling rate. In these cases, the ADCs is able to deliver an accuracy of about 12 bits when used on single ended channels. This would turn out in about $1.2 \cdot 10^{-4}$ relative uncertainty at full range, but such an uncertainty can be achieved only with a very low input impedance.

4. TEENSYDAQ BOARD AND EXTERNAL CONVERTERS

To overcome the performance degradation due to the low input impedance and the lack of active gain stages, the Author designed an advanced DAQ board with performance comparable to high-end commercial systems by adding some external active devices. Nevertheless, the cost of the new DAQ is of about 100 \$, still much lower than the price of competing products.

Figure 7 shows the general block diagram of the high performance DAQ. The new DAQ version still employs the Teensy 3.6, already used for the ultra-low-cost board. Such Teensy can be easily replaced with the Teensy 4.1 which features quite better performance with respect to Teensy 3.6 (larger RAM to store the data, higher clock frequency and improved processing capabilities). However, Teensy 4.1 lacks the DAC Converters and, therefore, it cannot be employed on the ultra-low-cost DAQ. The principal task of the Teensy is to interface the external ADC and DAC converters, to acquire and temporary store the data, and to send them to the host computer. Moreover, some optional signal processing (such as averaging and filtering) could be implemented on the Teensy itself thanks to its high computing capabilities.

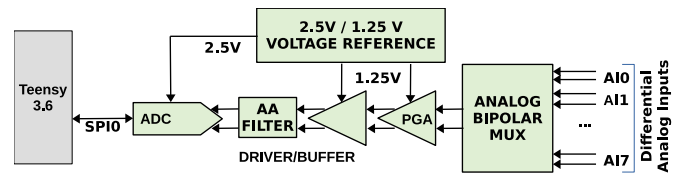


Figure 8. Block diagram of the analogue acquisition chain featuring the ADS8881 high-performance ADC.

The DAQ board is directly powered from the 5 V of the USB Port, therefore, no external power supply is required. However, internally the system needs different voltages for properly operating. For this reason, a dedicate power supply module, shown in Figure 7, is implemented in the DAQ. This module employs a boost/inverter DC-DC converter and few ultra-low-noise linear voltage regulators to provide the 15 V rails and the low-noise 3.3 V voltage required by the analogue inputs and outputs and the acquisition chain. Eventually, another 3.3 V voltage is generated by the Teensy and used to supply only digital circuits, avoiding any noise coupling between analogue and digital devices.

The overall performance and functionalities of this DAQ are comparable to, or even better than, many commercial boards which are available at a much higher cost.

4.1. Analogue Input Channels

The section related to the analogue input channels is highlighted with a green colour in Figure 7, while Figure 8 shows the detailed implementation of the ADC acquisition chain.

The DAQ features 8 fully differential inputs which can be alternatively used as single-ended inputs. Each channel has an input impedance higher than $1 G\Omega$ and all the channels can be sampled with a user-selectable sampling rate up to 1 Msample/s shared between the active channels. The acquisition of multiple channels is carried out sequentially by using an analogue multiplexer which features low noise, low distortion and high bandwidth.

A high-performance precision Programmable Gain Amplifier (PGA) is employed to maximize the input range capability of the acquisition chain. The PGA is connected to the multiplexer output and can be programmed to have 11 different gains in the range of $1/8 V/V$ to $128 V/V$. Additionally, the PGA can add an optional 1.375 gain factor. Therefore, thanks to the 22 different input gain combinations of the PGA, the DAQ is able to acquire analogue signals in bipolar ranges from about $\pm 19 mV$ up to about $\pm 12 V$. Moreover, the PGA is designed to add a fixed DC voltage to the output, so that the subsequent stages can be powered by a single-ended power supply.

The selected ADC is the Texas Instrument ADS8881 chip [20]. This high-performance ADC features a resolution of 18 bits and a maximum sampling rate of 1 MSample/s. It exhibits very good performance both in terms of linearity and accuracy when its inputs are properly decoupled and buffered. For this reason, a dedicated differential buffer/-driver with an anti-aliasing filter has been inserted between the PGA outputs and the ADC inputs. The topology selected for the anti-aliasing filter was a classic differential RC first-order low-pass filter.

Particular attention has been posed when designing the external voltage reference circuit required by the ADC. A high-accuracy and low-drift reference voltage with a nominal output value of 2.5 V was employed along with three operational amplifiers. In particular, the reference voltage selected for the

prototype was the REF5025I, featuring a low-noise output voltage of 2.5 V with an initial maximum uncertainty of 0.05 % and a temperature coefficient of only 3 ppm/°C. One high-speed operation amplifier is used as buffer for providing the reference voltage to the ADC. Such an amplifier satisfies the band and stability requirements of the ADC operating at its maximum frequency, but it does not have a suitable accuracy. To overcome such a problem, another high-accuracy operational amplifier has been inserted in the reaction chain of the first amplifier. This way all the ADC requests in terms of accuracy, band and stability are satisfied. A third high-accuracy operation amplifier is instead employed to generate a 1.25 V required for the proper operation of the PGA.

The data stream provided by the ADC is read by the Teensy 3.6 via the SPI0 interface and temporarily stored in the microcontroller RAM together with an accurate timestamp and a channel reference. Once acquired, the samples can be sent to the host PC via the USB Interface without any significant latency or sampling rate reduction. Optionally, the acquired data can be stored on the Micro Secure Digital (μSD) available on the Teensy. This is an added value of the proposed solution which can additionally operate as a standalone data logger without connection to any host computer. Of course, in this case, the DAQ board has to be powered by an external power source. As an example, a rechargeable battery can be employed making the DAQ a portable data logger able to operate also in remote locations.

4.2. Analogue Output Channels and Digital Input/Output

The DAQ can also be equipped with a maximum of four analogue output channels working with a resolution of 16 bits and a maximum sampling rate of 100 kHz, as highlighted in yellow in Figure 7. The outputs are capable of generating positive and negative voltages and currents in different ranges which can be selected by the user. These DACs can be used along with the input analogue channels and are able to generate arbitrary waveforms up to about 20 kHz. In this case, the waveform can be configured from the host PC and programmed into the Teensy, which will take charge to send the proper samples to the DACs without any user intervention.

Additionally, the board has 16 digital input/output channels (shown in orange in Figure 7) which are able to operate at 5 V. The channels can be read/written simultaneously in block of 8 bits and can be individually configured either as inputs or outputs. These digital channels are obtained by means of an IO Expander Chip which is connected to the Teensy 3.6 via the SPI2. Eventually, four high-speed digital inputs and four high-speed digital outputs are available as well. These digital lines are directly connected to the Teensy 3.6 IO Pins using a level converter which is able to operate with any logic level between 1.8 V and 3.6 V at a maximum frequency of 1 MHz.

The analogue outputs can be useful in several specific applications. As an example, they are able to accurately bias sensors such as load gauges and generate control signals for several systems. Moreover, together with the analogue inputs they can be used for implementing impedance measurements and readout units for electrochemical sensors. Eventually, the availability of digital lines allows the DAQ to interface with digital systems and they can be optionally used in PWM Mode.

4.3. High-Performance TeensyDAQ Characterisation

The design of the high-performance TeensyDAQ has been carried out trying to obtain an optimal trade-off among

performance, cost, size, and functions. Therefore, SMD packages have been selected both for performance and size constraints. Unfortunately, this can be an issue during the first testing stage of the prototype, being SMD devices more difficult to be handled and connected on development boards. For this reason, SMD-to-THT adapters, test jumpers, and sockets have been used to realize the first prototype of the board. This solution allows one to easily arrange/modify the circuits under test. However, the employment of wires and sockets severely degrades AC performance due to multiple noise coupling sources. Nevertheless, the Author tried to optimize the single blocks of the DAQ and carried out a preliminary characterisation of DC and AC performance, as described in the following sections, obtaining very promising results which are comparable with commercial high-end products.

4.4. DC performance

Initial tests have been carried out in order to assess DC accuracy and repeatability. All tests have been performed using as reference voltmeter the 8.5 digits HP 3458, calibrated less than 2 years ago with a stated DC uncertainty of less than 1 ppm. The ADC has been used at a sampling frequency of 100 kHz, acquiring about 30000 samples for each measurement (about 0.3 s measuring time). Initially, the complete acquisition chain has been verified (ADC together PGA and driver, see Figure 8) to observe linearity and overall gain of the DAQ.

Figure 9 shows the experimental results obtained in the input voltage range from -2.5 V to 2.5 V and setting the PGA gain to the unity. The plot inset shows an excellent linearity of the entire acquisition chain. The difference between the actual measured values and the expected ones is reported, as well. It is possible to see how the difference is extremely low with an overall gain very close to 1 and a negligible offset. Even though the measurement number is quite limited, it is possible to estimate the maximum linearity error for the entire measurement chain in about 200 μV, while maintaining mostly under 40 μV, as visible from Figure 9.

Then, acquisition chain noise and measurement repeatability have been assessed. The test has been carried out in three steps with the aim of quantifying the influence of each stage of the chain. Initially, the performance of only the ADC have been checked and compared with the specifications of the manufacturer. A stabilized power supply has been used to apply

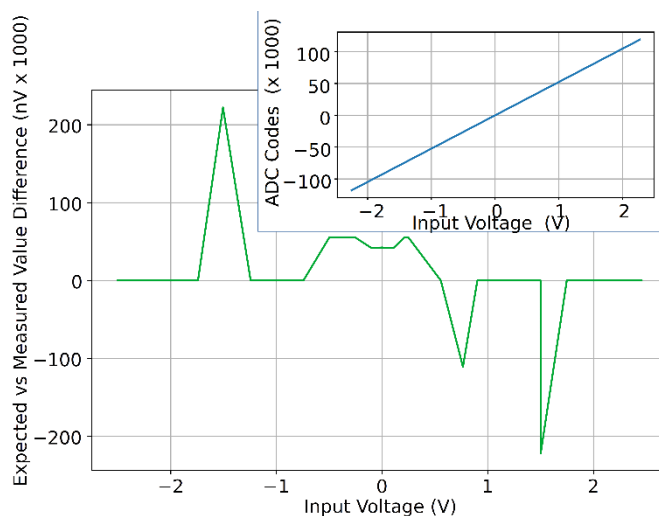


Figure 9. Transfer characteristic of the analogue acquisition chain obtained in an input voltage range of -2.5 V to 2.5 V by setting the PGA gain to 1 and the difference between expected and measured values.

voltages between -2.5 V and 2.5 V directly to the ADC input. Then, the same measurement has been repeated including the ADC Driver and the PGA. In particular, the input voltage has been measured at the same time with the DAQ and the HP 3458 voltmeter, acquiring respectively about 30000 and 20 measurements for each voltage. The standard deviation of the HP 3458 was negligible for all measurements.

Figure 10 shows the three sets of results: each dot shows the standard deviation obtained by the DAQ, respectively applying the input voltage to the ADC, to the ADC together with its driver, and to the whole acquisition chain (including the PGA). Of course, the lowest standard deviation is obtained with only the ADC, with a maximum value of about 35 ppm. It is worth to notice that 1 LSB at 18 bits resolution corresponds to 8 ppm. Therefore, the ADC standard deviation is of the order of 4 LSB, in-line with the 3 LSB declared by the manufacturer. The standard deviation slightly increases up to about 50 ppm when the ADC Driver is included, which corresponds to about 6 LSB. Eventually, the standard deviation reaches values of about 90 ppm when the complete acquisition chain is used. This increase is partially due to the intrinsic noise of the PGA, but also the presence of long connection wires which cannot now be neglected being the input impedance of the PGA higher than 1 G Ω .

Nevertheless, such results are extremely promising because in the same conditions several commercial high-end devices, available at much higher prices, have an uncertainty in the order of 3000 ppm without calibration and more than 100 ppm after calibration [21].

4.5. AC performance

Obtaining an AC characterisation of the DAQ is not straightforward. As an example, the DMM employed for the DC characterisation has an AC uncertainty of 10 ppm ~ 100 ppm depending on range and frequency, therefore, it is quite difficult to have a good Transfer Uncertainty Ratio.

For this reason, it has been decided to use a low-distortion sine generator and to compute the Fourier Transform of the acquired samples. The generator has a stated distortion of 0.01 % but it is not perfectly stable in frequency. Therefore, it is not possible to make the transform on an integer number of periods. Acquisitions have been carried out at nominal frequencies of

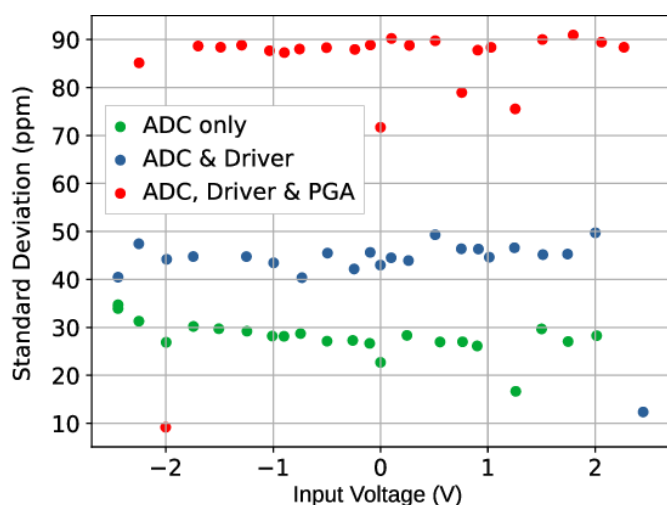


Figure 10. Standard deviation obtained from the proposed DAQ in the range from -2.5 V to 2.5 V, respectively considering the only ADC, the ADC together with its Driver, and the complete acquisition chain.

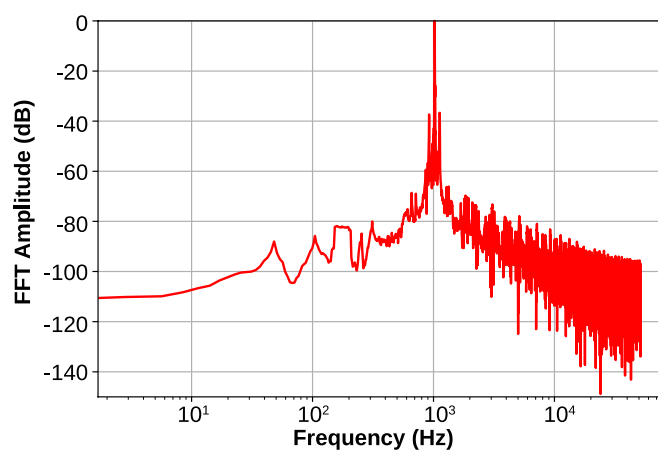


Figure 11. Fourier transform of the acquired data using 1 kHz sine input signal.

10 Hz, 100 Hz, 1 kHz and 10 kHz, while the ADC sampling frequency has been set to 100 kHz for all measurements. As an example, Figure 11 shows the result obtained with 1 kHz sine signal. It is possible to note the presence of high-frequency noise as well as components at 100 Hz and multiples, probably due to noise and mains coupling with the DAQ signal path. Notably, there are also two symmetrical lines around the main component at 1 kHz, probably due to the frequency instability of the signal generator. Nevertheless, the tail of the spectrum reaches -110 dB at low frequency and more than -90 dB at high frequency. Therefore, the achieved performance is generally quite promising, also considering that the assembly of this first prototype has multiple noise-coupling paths due to several wired connections and sockets between the DAQ components.

5. CONCLUSIONS

The paper presents the design and initial characterisation of two DAQ multi-platform solutions with the aim of addressing several issues currently present on most of the commercial devices: software/hardware limited compatibility and support, high cost and impossibility to freely modify the software to fit any specific applications. The two boards are based on a Teensy 3.6 and are able to operate on most of the operative systems thanks to a dedicated software infrastructure designed to simplify the use, the maintenance and the upgrading.

The first version is very simple and employs only the Teensy 3.6 and few passive devices. It features an extremely low-cost of about 30 \$, but it has quite limited performance and can be employed only when the input signal impedance is very low.

The second version, instead, uses external high-performance ADC and DACs converters and is able to achieve performance comparable with high-end commercial products, but at a cost anyway lower than 100 \$. The first prototype of the DAQ has been tested and several optimizations have been carried out. The achieved results are very interesting and demonstrate the feasibility of the proposed board as an alternative solution to commercial products. Nevertheless, due to circuit assembly implemented by using sockets and several connection wires, the AC performance requires further investigation. For this reason, a new prototype is currently under development. The new board will be realized using printed circuit boards in a modular design, where each block (as shown in Figure 7) will be implemented as an independent module so that it will be very easy to change or upgrade any part of the system.

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