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Lock-in amplifier with a high common-mode rejection ratio in the range of 0.02 to 100 kHz

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ABSTRACT
The paper presents a new lock-in amplifier with a differential input. The lock-in amplifier has a high common-mode rejection ratio of 200 dB at 1 kHz and 160 dB in the frequency range of 20 Hz to 100 kHz. A method for extending the dynamic range of comparing signals is suggested. The experimental results of metrological characteristic tests are discussed.

Section: RESEARCH PAPER

Keywords: lock-in amplifier; differential input; voltage dividers; common-mode rejection ratio; calibration

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1. INTRODUCTION

One of the classic problems of instrumentation is the comparison of alternating voltage amplitudes [1]-[4]. Inductive voltage dividers (IVDs) are usually used for precision AC [5]-[11]ratio measurements. To calibrate IVD ratio K_{IVD} errors, the calibrated IVD referencing method is the most widely used [12], [13]. For example, this method is used in the National Institute of Standards and Technology (NIST, USA) to calibrate decade IVDs (54120C – 54131C services) in the range of 50 Hz to 20000 Hz [14]. In the calibration process, an IVD ratio is compared with a ratio from a reference IVD using the differential method of measurement. Comparisons of two AC voltages $v_x(t)$ and $v_0(t)$ with the same frequency ω lock-in amplifiers with a differential input (LIADI) are usually applied. [15], [16]. LIADI defines the measurement precision and permits the separation of a low differential signal from a high common-mode interfering signal.

A block diagram of a measuring IVD ratio error using the LIADI system is shown in Figure 1.

Figure 2 shows a block diagram of a simple LIADI. According to the scheme, the amplitudes of in-phase signals $v_x(t)$ and $v_0(t)$ are compared, the signal is then amplified and the signal difference detected.

Lock-in amplifiers are mainly used in physical and chemical sensing applications [17]-[26]. However, LIADI inputs are also used for calibration measurement instruments [15], [16], [27].

Equation (1) below defines the output voltage of simple LIADI (Figure 2):

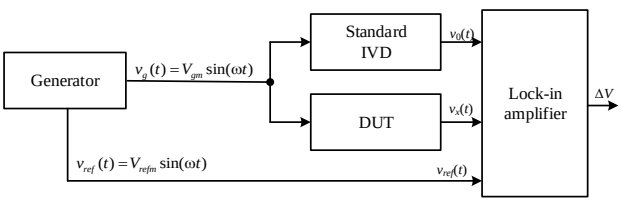

Figure 1. Block diagram of a measuring IVD ratio error system.

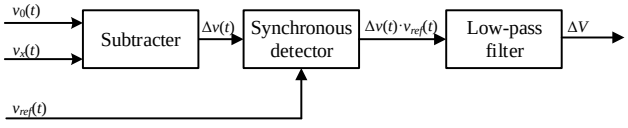

Figure 2. A simple lock-in amplifier with a differential input (a basic LIADI).

$$\Delta V \approx \frac{1}{U}\left(\frac{1}{2\pi}\int_0^{\infty}\left[v_x(t)-v_0(t)+\frac{v_x(t)+v_0(t)}{2CMRR}\right]v_{ref}(t)dt\right);$$
$$v_x(t)=V_{xm}\sin(\omega t+\varphi_x);$$
$$v_0(t)=V_{0m}\sin(\omega t+\varphi_0); \quad (1)$$
$$v_{ref}(t)=V_{refm}\sin(\omega t+\varphi_{ref}),$$

where U is the multiplier denominator voltage, V; V_{0m} and V_{xm} are the compared signals amplitudes, V; V_{refm} is the reference voltage; V; φ_0, φ_x, are the compared signal phases, rad; φ_{ref} is the reference signal phase, rad; and *CMRR* is the common-mode rejection ratio.

As shown in equation (1), the signal amplitude difference ΔV has an error that depends on the phase shifts of the input signals φ_x, and φ_0 is a common-mode rejection ratio and phase shift of reference signal φ_{ref}.

[16] and [27] explain the possibility of reducing the error of measuring the absolute difference between the compared voltages induced by a phase error.

In this current work, methods of reducing the error-conditioned measurements by using the finite value of the common-mode rejection ratio in a LIADI are suggested. A new circuit is proposed for the input stage of the LIADI input based on an instrumentation amplifier and a voltage follower.

2. THE COMMON-MODE REJECTION RATIO FOR IVDS

Requirements for the common-mode rejection ratio can be improved, specifically when the verification and calibration of the IVD at a 1-10 nV maximum resolution of the lock-in amplifier within the medium frequency range at the upper level of $10\sqrt{2}$ V of the compared voltage dynamic range [28]-[30].

The instrumentation amplifier application is the standard method for input differential signal extraction.

The output voltage is determined by equation (2) because its response delay can be neglected in frequency range

$$V_{out} = A_d V_d + A_c V_c = A_d\left(V_d + \frac{V_c}{CMRR}\right), \quad (2)$$

where A_d is the differential-mode gain; A_c is the common-mode gain; V_d is the differential voltage, V; and V_c is the common-mode voltage, V.

The finite value of *CMRR* is determined by the value of relative error γ_c. In this case, the ultimate requirements for *CMRR* are

$$CMRR = \frac{V_c}{\gamma_c V_d}. \quad (3)$$

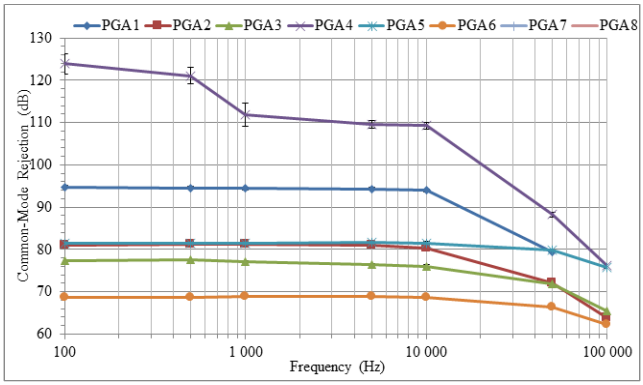

Figure 3. Results of experimental studies concerning the PGA207 instrumentation amplifier.

According to equation (3), the common-mode rejection is (200–220) dB at γ_c = 0.1, but it is not realised in commercially available lock-in amplifiers. Other important characteristics of a lock-in amplifier that must be taken into account are the bandwidth, high input impedance at measurement inputs, high stability, and low nonlinearity of the differential signal gain.

For example, one of the best commercially available lock-in amplifiers, SR830 of Stanford Research Systems, has a common-mode rejection of 100 dB up to 10 kHz, decreasing by 6 dB per octave above 10 kHz, and an input impedance 10 MOhm//25 pF [31]. In [32], a special guarded vector voltmeter (a lock-in amplifier) with a bootstrapping-guarding technique [33] is proposed for the calibration of the IVD. It has a high common-mode rejection of 180 dB at 1 kHz. With our IVD [28], we must compare voltages of up to $10\cdot\sqrt{2}$ V with a resolution of up to 10 nV at a frequency of 1 kHz. Therefore, by means of the lock-in amplifier, a common-mode rejection of about 200 dB should be obtained.

We suggest the use of the instrumentation amplifier in its integrated form with a programmable gain ratio for IVD comparison. In such amplifiers, *CMRR* does not depend on the output impedance of the compared signal sources because its dependence on the internal impedances of the cascaded instrumentation amplifier is technologically minimised. After analysing the parameters of the different instrumentation amplifiers performed for the differential signal extraction, Texas Instrument PGA207 has been chosen [34].

However, PGA207 and similar amplifiers have a low common-mode rejection of 100 dB at A_d = 10. Experimental studies of *CMRR* on eight PGA207 samples were carried out. Equal values of voltage (5 V) were applied to both the PGA207 inputs, and the value of voltage ΔV by the lock-in amplifier SR830 was measured on the PGA207 output at A_d = 10.

All tests were undertaken three times for each frequency at an environment temperature of 22±2 °C. The common-mode signal rejection ratio was calculated by

$$CMRR = 20\lg\frac{5}{\Delta V}, \quad (4)$$

The results of the experimental studies (Figure 3) of the PGA207 instrumentation amplifier have confirmed the low value of the common-mode rejection ratio and have shown significant dispersion of the common-mode rejection ratio from sample to sample.

In summary, it has been shown, both theoretically and empirically, that the circuit technique must be used for further increasing the common-mode rejection.

3. APPLICATION OF TRACKING POWER SUPPLY TO DIFFERENTIAL SIGNAL EXTRACTION

The common-mode rejection in lock-in amplifiers can be increased by the addition of the voltage follower to the scheme, as shown in Figure 4, which provides the tracking power supply of the instrumentation amplifier.

The efficient common-mode rejection ratio is

$$CMRR_{ef}(t) = \frac{CMRR(t)}{1-A_f(t)}, \quad (5)$$

where $A_f(t)$ is the voltage follower voltage gain.

The common-mode rejection decrease to 160-180 dB can be achieved within the frequency range of practically inertialess

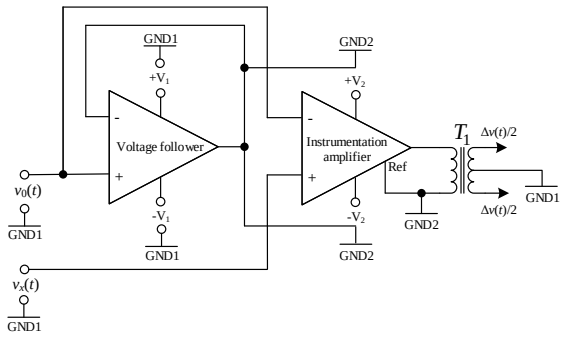

Figure 4. Differential signal extraction scheme.

circuits at easily reachable values of 0.999-0.9999 of the voltage follower voltage gain.

This approach has serious disadvantages. The transmission factor module of the voltage follower and the instrumentation amplifier decreases with the increase in frequency, resulting in the *CMRR* of the whole circuit [35].

Thus, we can see the high rejection of the common-mode signal only in the narrow frequency band.

Tracking a power supply circuit with the use of a voltage follower also provides an increase in the input impedance of the measuring channels in the wide frequency range, especially the v_x channel of the instrumentation amplifier.

Figure 5 shows the novel technical implementation of the input stage of the lock-in amplifier that is used for tracking the symmetrical power supply of the instrumentation amplifier. The connection circuit of the instrumentation amplifier is presented in Figure 6.

The high-quality operating amplifier (DA_1) in the voltage follower circuit, as shown in Figure 5, must be used to solve the posed problem.

This amplifier is provided with an acceptable voltage profile of no less than ±18 V of the tracking symmetrical power supply and is presented by OP285. A conventional representation (Figure 5) of the uncomplemented input supply of this amplifier is conditioned by means of the flexible diode protection circuit of the voltage follower inputs in a number of cases so as to provide its normal quiescent mode at the disconnection of a signal source.

The effect of cable capacitance is reduced due to the suspension of their braiding to the voltage follower input (Figure 6).

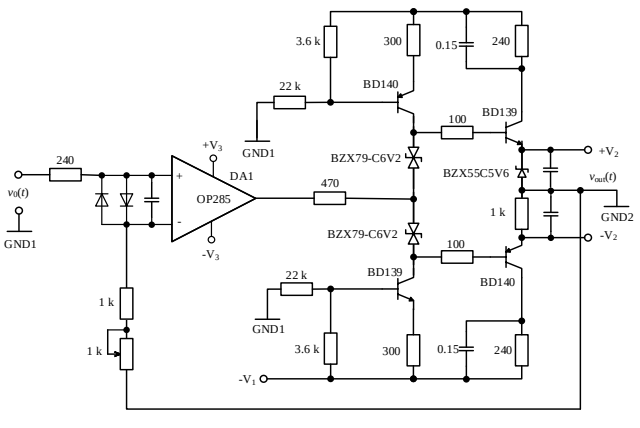

Figure 5. Voltage follower circuit for tracking power supply formation.

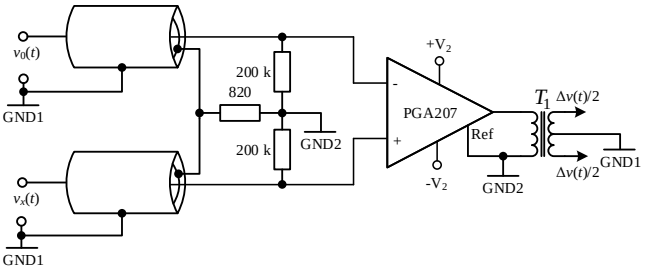

Figure 6. Connection circuit of the instrumentation amplifier.

As shown in Figure 6, the output signal is to be obtained relative to the original ground. It can be carried out, at least, by using optical or transformer isolation. The first method leads to an abrupt loss of sensitivity due to the properties of diode optrons. Therefore, the second method is more expedient.

4. INVESTIGATION OF THE DIFFERENTIAL SIGNAL EXTRACTION CIRCUIT

The differential signal extraction circuit (see Figure 5 and Figure 6) was simulated in the Multisim software, applying common-mode input signals with amplitudes $V_{0m} = V_{xm} = 10 \cdot \sqrt{2}$ V. The frequency dependences of the *CMRR* from $|A_f(f)|$, phase $A_f(f)$, and output voltage amplitude $|\perp v(f)|$ were estimated. The results of the simulation are shown in Table 1.

The proposed circuit permits increasing the common-mode rejection up to 141 to 220 dB at a frequency range of up to 100 kHz (see Table 1).

The obtained resolution is <1 nV in the frequency range of up to 10 kHz, <10 nV in the frequency range of up to 20 kHz, <100 nV in the frequency range of up to 60 kHz, and <1000 nV in the frequency range of up to 100 kHz.

The differential signal extraction circuit implementation is shown in Figure 7. The experimental investigation setup for the differential signal extraction circuit is shown in Figure 8.

The CH0 output of the Fluke 5520A calibrator supplied a voltage of $10 \cdot \sqrt{2}$ V and a frequency of 1 kHz. The same signal was applied to the DI-3m [28] inductive divider with a ratio of 0.100000. The $\perp V$ values were measured at the lock-in amplifier SR830 resolution up to 2 nV, five times for 35 different frequencies (Figure 8).

Table 1. Results of the differential signal extraction circuit simulation.

Frequency (Hz)	$\|A_f(t)\|$	Phase of $\|A_f(t)\|$ (deg)	$\|\Delta v(t)\|$ (V)	CMR (dB)
100	1.000001	$-0.84 \cdot 10^{-6}$	$1.01 \cdot 10^{-10}$	220
1000	1.000002	$-8.67 \cdot 10^{-6}$	$2.01 \cdot 10^{-10}$	214
10000	1.000003	$-83.1 \cdot 10^{-6}$	$1.01 \cdot 10^{-9}$	200
20000	1.000010	$-161 \cdot 10^{-6}$	$6.57 \cdot 10^{-9}$	184
30000	1.000021	$-201 \cdot 10^{-6}$	$1.91 \cdot 10^{-8}$	174
40000	1.000037	$-137 \cdot 10^{-6}$	$4.11 \cdot 10^{-8}$	168
50000	1.000048	$112 \cdot 10^{-6}$	$6.97 \cdot 10^{-8}$	163
60000	1.000062	$783 \cdot 10^{-6}$	$1.05 \cdot 10^{-7}$	160
70000	1.000065	$1.84 \cdot 10^{-3}$	$1.44 \cdot 10^{-7}$	157
80000	1.000058	$3.79 \cdot 10^{-3}$	$2.07 \cdot 10^{-7}$	157
90000	1.000040	$6.42 \cdot 10^{-3}$	$4.85 \cdot 10^{-7}$	146
100000	1.000016	$11.5 \cdot 10^{-3}$	$8.89 \cdot 10^{-7}$	141

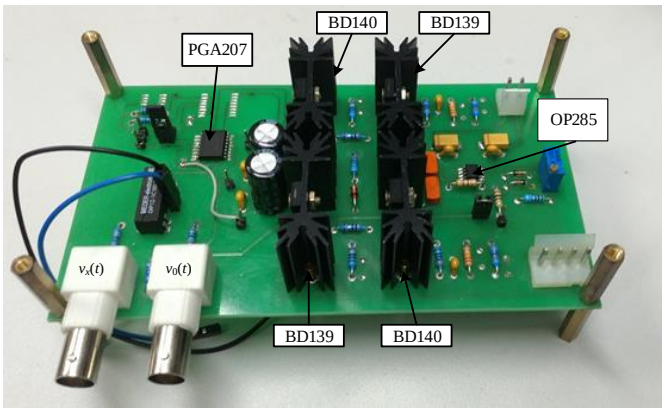

Figure 7. A photo of the differential signal extraction circuit implementation.

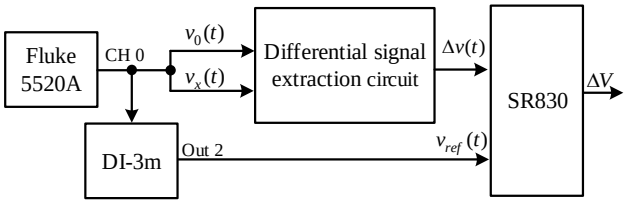

Figure 8. Experimental investigation setup.

The common-mode rejection of the differential signal extraction circuit is calculated as

$$CMRR = 20\lg\frac{10\sqrt{2}}{\Delta V}, \quad (6)$$

where $10\sqrt{2}$ is calibrator Fluke 5520A nominal voltage, V.

Figure 9 shows the implementation of the differential signal extraction scheme that allows us to increase the common-mode rejection up to 100 to 190 dB at a frequency range of up to 100 kHz. The obtained maximum resolution is <10 nV in the frequency range of up to 1 kHz.

The sample and hold circuit can be added to the lock-in amplifier for achieving the required common-mode rejection. One of the technical realisations of the sample and hold circuit for the lock-in amplifier us described in [35]. Experimental investigations for differential signal extraction circuit with sample and hold circuit [35] are also provided by the scheme shown in Figure 8. The results of the differential signal extraction circuit experimental investigation with sample and hold circuit are shown in Figure 10.

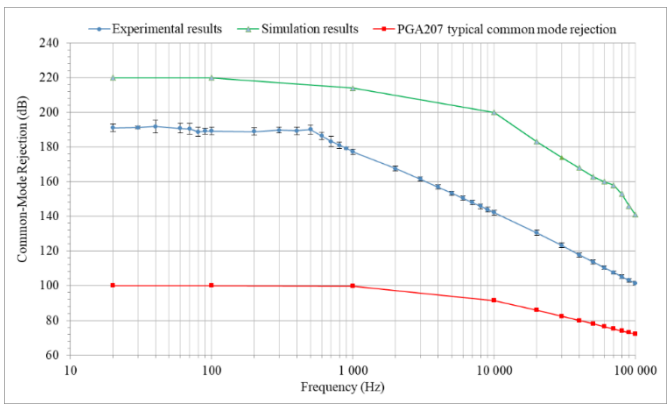

Figure 9. Results of the differential signal extraction circuit experimental investigation.

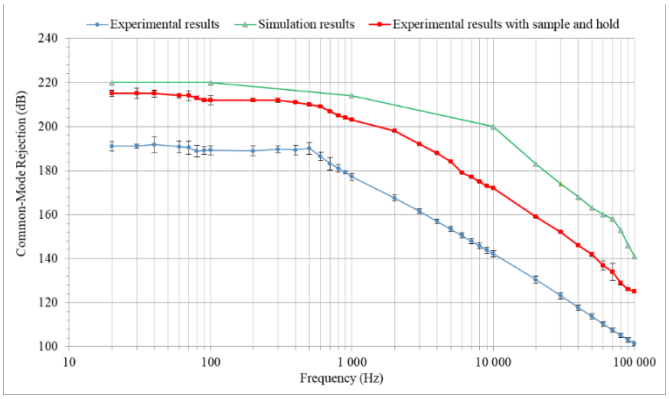

Figure 10. Results of the differential signal extraction circuit experimental investigation with sample and hold circuit.

Figure 10 shows the implementation of a differential signal extraction circuit with sample and hold circuit, which allows us to increase the common-mode rejection up to 125 to 215 dB in a frequency range of up to 100 kHz. The obtained maximum resolution is < 1 nV in the frequency range of up to 1 kHz and < 10000 nV in the frequency range of up to 100 kHz.

5. NEW LIADI

5.1. Block schematic

The new LIADI structure, which uses a developed differential signal extraction circuit with sample and hold circuit, is introduced. A block diagram of the new LIADI is shown in Figure 11.

The LIADI consists of a voltage follower (VF); an instrumentation amplifier (IA); a programmable gain amplifier (PGA), a synchronous detector (SD); a low-pass filter (LPF); a sample and hold device (SH); an analogue-to-digital converter (ADC); and a microcontroller (MC).

The VF is assembled on the OP285 and PGA207 ICs; the PGA207 also accommodates IA, PGA, and SH. The synchronous detector is based on the AD734 IC, and its denominator voltage is set close to 1 V for improved sensitivity [36]. The LPF has a cut-off frequency of 0.2 Hz and is based on the OP270 IC. To achieve a uniform transient response, we use a third-order Bessel filter.

The LIADI can automatically be calibrated to reduce the effect of a residual in-phase component on the LPF output. To calibrate, the same voltage $v_0(t)$ is applied on both the inputs of the differential signal extraction scheme (Figure 4). The output voltage is stored in the SH and serves as a correction during measurements.

The ADC is assembled on the MAX110 IC. An MC (ATmega128) controls the operation of the LIADI's PGA, implements an additional digital filter, and indicates the measurement results.

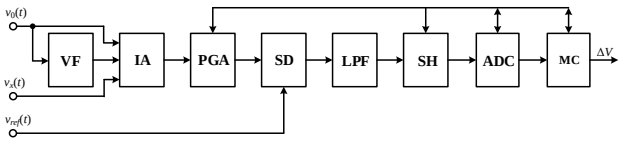

Figure 11. New LIADI block diagram.

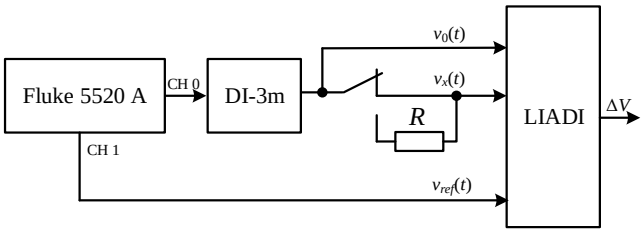

Figure 12. Diagram of the setup to measure the V_x channel input resistance of the LIADI.

Table 2. Calculation data on input resistances.

Resistor *R*	Indicator reading, (μV)	Input resistance, (MΩ)
In circuit V_0	5	200
In circuit V_x	-0.5	2000

5.2. LIADI input resistance

The characteristics of the LIADI are measured experimentally using the DI-3m [28] reference divider. The DI-3m has auxiliary and main outputs connected to the output of the first decade (Out.1) and the minor decade (Out.2).

A V_x channel input resistance was determined using the Fluke 5520 A calibrator with a two-step indirect measurement method (Figure 12). The calibrator's main (CH0) and auxiliary (CH1) outputs supplied the 1 kHz sinusoidal voltage of 10√2 V and 5√2 V, respectively. The ratio K_{IVD} of the DI-3m was set to 0.100000.

First, the same signal was applied to the V_0 and V_x inputs to calibrate the LIADI. Second, the input V_x was connected via a precision reference resistance *R* of 1 kΩ (USF340 1.00K 0.01 % 5 ppm/°C [37]), and the voltage difference ΔV was recorded according to the data provided by the LIADI indicator.

The LIADI input resistance was calculated according to

$$R_{IN} = \frac{V_{IN} K_{IVD}}{|\Delta V| / R}, \tag{7}$$

where V_{IN} is the calibrator output voltage CH0, *V*.

The V_0 channel-based input resistance was determined in a similar way, connecting the input V_0 via reference resistor *R*. The difference in voltages ΔV was recorded.

The calculated input resistances are given in Table 2.

5.3. The LIADI resolution

The LIADI resolution was determined according to the scheme shown in Figure 13.

To measure the LIADI resolution, the indirect measurement method was used. The IVD DI-3m working calibration standard was used to set up nominal voltage V_{DI3m} between outputs 1 and 2. The voltage difference ΔV was recorded according to the data provided by the LIADI indicator.

The CH0 and CH1 outputs of the calibrator supplied

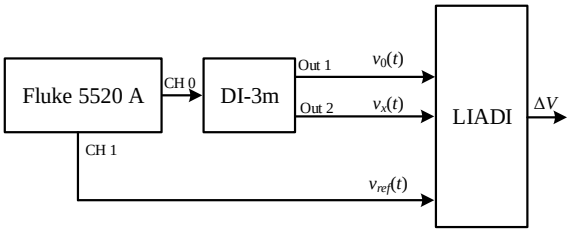

Figure 13. Diagram of the setup for resolution measurement.

Table 3. LIADI resolution.

Out-of-balance voltage in μV	LIADI output Δ*U* in μV	Relative reading deviation *γ* in %
LIADI resolution of 10 μV		
100	100	< 0.5
200	200	< 0.3
300	300	< 0.2
400	400	< 0.2
500	500	< 0.1
LIADI resolution of 1 μV		
10	10	< 5.0
20	20	< 2.5
30	30	< 1.7
40	40	< 1.3
50	50	< 1.0
LIADI resolution of 100 nV		
10	10.1	1.0
20	20.4	2.0
30	30.7	2.3
40	41	2.5
50	51.2	2.4
LIADI resolution of 10 nV		
10	10.21	2.1
20	20.34	1.7
30	overload	-

voltages of 10√2 V and 5√2 V, respectively, with a frequency of 1 kHz. The DI-3m ratio of output 1 was set to 0.100000. To determine resolutions 10 nV, 100 nV, and 1 μV, the IVD ratio of output 2 was varied in the range of 0.100001 to 0.100005. To determine resolution 10 μV, the IVD ratio of output 2 was varied in the range of 0.100010 to 0.100050. The LIADI relative deviation was calculated according to

$$\gamma = \frac{\left(V_{DI3m} - \Delta V\right)}{V_{DI3m}} \cdot 100, \tag{8}$$

where V_{DI3m} is the IVD DI-3m nominal voltage between outputs 1 and 2, *V*. The results of the measurements are presented in Table 3.

5.4. LIADI dynamic range

The dynamic range of the compared voltages was defined according to the scheme shown in Figure 13. Again, the CH0 and CH1 outputs of the calibrator supplied voltages of 10√2 V and 5√2, respectively, with a frequency of 1 kHz. The DI-3m ratio of output 1 was set to 0.999999. The IVD ratio of output 2 was varied in the range of 0.999998 to 0.999994. ΔV values were measured at the LIADI resolution of 100 nV. The LIADI relative deviation was calculated according to equation (8).

The minimum amplitude of the compared voltages was determined with similar calibrator settings. The DI-3m ratio of output 1 was set to 0.000000. The IVD ratio of output 2 was varied in the range of 0.000001 to 0.000005. ΔV values were measured at the LIADI resolution of 100 nV. Again, the LIADI relative deviation was calculated according to equation (8).

The results of the measurements are presented in Table 4.

Table 4. Maximum and minimum amplitude of the LIADI.

Out-of-balance voltage in µV	LIADI output Δ*V* in µV	Relative reading deviation *γ* in %
Maximum amplitude		
10	10.2	2.0
20	20.3	1.5
30	30.6	2.0
40	40.7	1.8
50	51.1	2.2
Minimum amplitude		
10	10.1	1.0
20	20.2	1.0
30	30.4	1.3
40	40.8	2.0
50	50.9	1.8

5.5. LIADI frequency range

The frequency range of the compared voltages was defined according to the scheme in Figure 14. Again, the CH0 output of the calibrator supplied a voltage of 10√2 V with a frequency of 1 kHz. The same signal was applied to the second DI-3m IVD2 with a ratio of 0.500000. The IVD1 ratio of outputs 1 and 2 was set to 0.100000 and 0.100005, respectively, to compare the voltage amplitude of about 1√2 V. The $\sphericalangle V$ values were measured at the LIADI resolution of 100 nV for ten different frequencies (Table 5).

The relative frequency deviation of the LIADI readings was calculated accordingly:

$$\gamma_f = \frac{\left(\Delta V_{f(1)} - \Delta V_f\right)}{\Delta V_{f(1)}} \cdot 100, \tag{9}$$

where $\sphericalangle V_{f(1)}$ and $\sphericalangle V_f$ are IVD out-of-balance voltages at frequencies of 1 kHz and *f*, *V*.

Next, we set the IVD1 ratio of outputs 1 and 2 to 0.001000 and 0.001005, respectively, to compare the voltage amplitude of about 0.01√2 V. The measurements were repeated.

The results of the frequency range measurements are given in Table 5.

The measurements show that for all of the frequency range of 0.02 to 100 kHz, the relative error of comparison is less than 5 % (Table 5).

5.6. LIADI common-mode rejection

The common-mode rejection was defined according to the scheme in Figure 15. Again, the CH0 output of the calibrator supplied a voltage of 10√2 V with a frequency of 1 kHz. The same signal was applied to the DI-3m with a ratio of 0.500000. The $\sphericalangle V$ values were measured at the LIADI resolution of

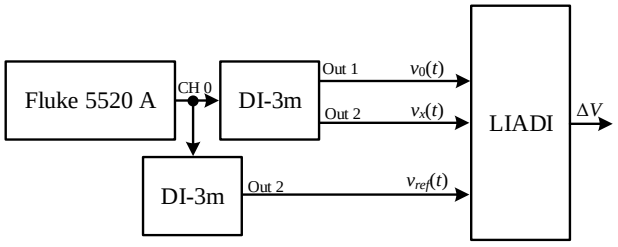

Figure 14. Diagram of the setup for measurement of the frequency range.

Table 5. Frequency range.

A voltage comparison at voltage amplitude of 1√2 (V)										
Frequency in kHz	1	0.2	0.08	0.04	0.02	10	20	40	80	100
IVD out-of-balance voltage in µV	51.3	50.3	49.9	48.7	48.9	53	50.3	50	48.9	48.8
Error in %	–	1.9	2.7	5.0	4.7	3.3	1..9	2.5	4.7	4.9
A voltage comparison at voltage amplitude of 0.01√2 (V)										
IVD out-of-balance voltage in µV	50.5	50.1	49.7	48.8	48.5	52.7	51	51	48	48.2
Error in %	–	0.8	1.6	3.4	4.0	4.3	1.0	1.0	4.9	4.5

10 nV for 20 different frequencies (Table 6).

The common-mode rejection of the LIADI was calculated according to equation (6).

6. CONCLUSION

In this article, we have proposed a new scheme for a lock-in amplifier with a differential input, LIADI. The amplifier is based on two instrumentation amplifiers and a voltage follower and has a common-mode rejection that is better than 200 dB at

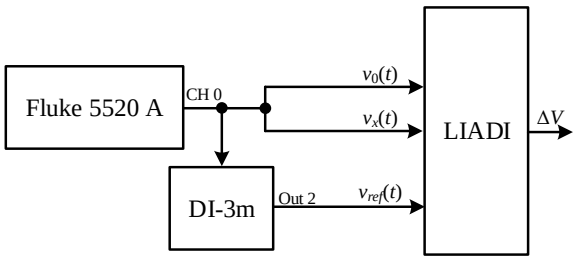

Figure 15. Diagram of the setup for measurement of the common-mode rejection ratio.

Table 6. Common-mode rejection ratio.

Frequency in kHz	LIADI output Δ*V* in nV	*CMR* in dB
0.02	< 10	> 200
0.04	< 10	> 200
0.06	< 10	> 200
0.08	< 10	> 200
0.1	< 10	> 200
0.2	< 10	> 200
0.4	< 10	> 200
0.6	< 10	> 200
0.8	< 10	> 200
1.0	< 10	> 200
2	< 10	> 200
4	< 10	> 200
6	< 10	> 200
8	< 10	> 200
10	< 10	> 200
20	10	> 200
40	40	> 180
60	90	> 180
80	210	> 160
100	820	> 160

1 kHz and greater than 160 dB in the frequency range 20 Hz to 100 kHz. The amplifier has a high input impedance of 2000 MOhm and 200 MOhm for V_X and V_0 inputs, respectively.

The new LIADI has the following characteristics:

- Frequency range: 0.02 to 100 kHz
- Input voltage range: 10√2 μV to 10√2 V
- Voltage resolution: 10 nV at a frequency of 1 kHz
- Resolution: 100 nV, 1 μV and 10 μV.

The developed LIADI is used to measure harmonics in planar fluxgate sensors. It is also used to calibrate the IVD ratio at Tomsk Polytechnical Univesity and at the All-Russian Scientific Research Institute of Physical and Radio Technical Measurements (VNIIFTRI, Moscow).

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