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Implementation of 20 nm Graphene Channel Field Effect Transistors Using Silvaco TCAD Tool to Improve Short Channel Effects over Conventional MOSFETs

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Abstract

In recent years, demands for high speed and low power circuits have been raised. As conventional metal oxide semiconductor field effect transistors (MOSFETs) are unable to satisfy the demands due to short channel effects, the purpose of the study is to design an alternative of MOSFETs. Graphene FETs are one of the alternatives of MOSFETs due to the excellent properties of graphene material. In this work, a user-defined graphene material is defined, and a graphene channel FET is implemented using the Silvaco technology computer-aided design (TCAD) tool at 100 nm and scaled to 20 nm channel length. A silicon channel MOSFET is also implemented to compare the performance. The results show the improvement in subthreshold slope (SS) = 114 mV/dec, I_{ON}/I_{OFF} ratio = 14379, and drain induced barrier lowering (DIBL) = 123 mV/V. It is concluded that graphene FETs are suitable candidates for low power applications.

Keywords: graphene, MOSFET, Silvaco TCAD, graphene FET, 2D low power design, 2D-material

1. Introduction

Conventional metal oxide semiconductor field effect transistors (MOSFETs) have a limitation when scaled down to nanometer channel lengths. Their performance is degraded and short channel effects emerge, which degrade the overall performance of devices. The circuit designed using the scaled device consume more static and dynamic power. Hence, the era of conventional MOSFETs has come to an end and the device design community is in search of an alternative of conventional MOSFETs. It is important to search for a convincing material, which can be used at small channel lengths. Graphene is a promising material due to its higher mobility, better electrical conductivity, and better thermal conductivity. The implementation of this atomically thin material needs to be defined in the Silvaco technology computer-aided design (TCAD) tool for any further use of graphene material applications.

The purpose of this study is to investigate and use the significant properties of the promising graphene material as a channel to replace conventional MOSFETs. The mobility of graphene material is high, and hence it can be used as a channel material for small geometry devices. The work on graphene channel FETs is still in its initial stage, as it needs to further improve and optimize the I_{ON}/I_{OFF} ratio, subthreshold slope (SS), and drain induced barrier lowering (DIBL) of these short channel parameters. In the present scenario, graphene FETs are the demanding devices for low power, radio frequency (RF),

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biosensor circuits, and high-speed analog very-large-scale integration (VLSI) designs. One major concern for designing graphene FETs is the availability of software tools because graphene is not available in conventional TCAD tools such as the Silvaco TCAD and Synopsys Sentaurus TCAD tools. Hence, one purpose of the study is to add graphene as a user-defined material in the Silvaco TCAD tool, which can be used for any applications.

The study is organized as follows. Section 2 presents the detailed literature review. Section 3 describes the design methodology used for implementation. Section 4 provides the design of 100 nm FET using silicon and graphene material channels, defining the graphene material in the Silvaco TCAD tool. Section 5 discusses the scaling of the device to 20 nm FET using silicon and graphene material channels. Section 6 focuses on the results and the comparison with other published results. Finally, the study is concluded.

2. Literature Review

In 2015, International Technology Road Map for Semiconductors (ITRS) discussed various emerging transistor structures in nano-scales [1]. Graphene FETs are one of the suitable candidates for future high-density and high-speed circuits [2]. Graphene FETs are designed by using top gate, bottom gate, and side gate approach to improve device parameters. Various substrate materials like silicon substrates, SiC substrates, and hexagonal boron nitride (hBN) substrates are reported as per the study. A bi-layer graphene sheet or graphene nanoribbon (GNR) is used to introduce the bandgap in a graphene FET due to which it becomes a suitable candidate for digital applications [3]. Initially, Novoselov et al. [4] extracted graphene from carbon and proposed that graphene could be the best possible metal for FET applications. In addition to the scalability to true nanometer sizes, graphene also offers linear current-voltage (I-V) characteristics, ballistic transport, and huge sustainable currents (9108 A/cm^2). Graphene transistors show a rather modest on-off resistance ratio, which is a natural drawback of a material having zero bandgaps [4]

Schwierz [5] focused on graphene transistors' status, prospects, and problems. The author reported the classification and detailed analysis of various graphene transistors developed in recent years. The challenge of graphene FETs is the opening of the bandgap of the defined size and the reliable approach compatible with standard semiconductor processing steps. For logic operations, a bandgap of 0.4 eV or more will be required [5]. Marmolejo-Tejada et al. [6] presented a study of GNR based FETs. The authors concluded that GNR-FETs can be used for switching applications, and can offer a high I_{ON}/I_{OFF} ratio and the SS near its ideal value [6]. Chen et al. [7] proposed a simulation program with integrated circuit emphasis (SPICE) compatible model of MOS type GNR-FETs with doped reservoirs, currents, and charge models which closely match with numerical TCAD simulations. They observed that GNR-FETs are promising compared to silicon complementary metal oxide semiconductors (CMOS) since these devices have either lower power or lower delay. GNR-FETs are still promising candidates for low-power applications [7].

Chen et al. [8] proposed a bi-layer graphene-based electrostatically doped tunnel field effect transistor (BED-TFET), and studied the operation principle of the BED-TFET and its performance sensitivity to the device design parameters. Agarwal et al. [9] proposed a bi-layer graphene tunneling field effect transistor (BLG-TFET) suitable for digital CMOS logic circuits. A bandgap opening is induced in BLG using both top-bottom asymmetric chemical doping and vertical electric field. The proposed BLG-TFET shows better characteristics for ultralow-power applications, specifically in low to medium-speed applications [9]. Lv et al. [10] proposed segmented edge saturation (SES) as a novel method to design high-performance TFETs using smooth GNR. Both high on-to-off current (I_{ON}/I_{OFF}) ratio and large I_{ON} are obtained [10].

Rassekh and Fathipour [11] reported a junctionless transistor (JLT) at 10 nm gate length, which is suitable for low power applications. The authors reported few parameters, i.e., I_{ON}/I_{OFF} ratio = 4.2×10^4, threshold voltage (V_{th}) = 327 mV, DIBL = 218 mV/V, SS = 109.9 mV/dec., and the comparison is carried out with silicon-on-insulator (SOI) fin-shaped field effect

transistors (FinFETs) [11]. Boukortt et al. [12] reported a SOI n-channel FinFET using the Silvaco tool at 8 nm gate length, and demonstrated the effects of gate work function on various parameters. The authors reported few parameters such as SS = 63.13 mV/dec, I_{ON}/I_{OFF} ratio = 10^6, and DIBL = 85.30 mV/V [12]. Pravin et al. [13] demonstrated the effectiveness of using a high-k dielectric material. The authors used HfO_2 material as dielectrics instead of SiO_2. These authors observed that DIBL is reduced by 61.5%, delay is reduced by 4%, and I_{ON}/I_{OFF} ratio is equal to 10^9.[13]. Ning et al. [14] demonstrated a flexible FET using the chemical vapor deposition (CVD) technique. The proposed FET exhibits I_{ON}/I_{OFF} ratio = 400 on a bending surface [14].

He et al. [15] studied the temperature effect on graphene FETs for RF applications. The authors found that graphene FETs could be used up to 200℃ temperature using SiC substrates [15]. Tamersit and Djeffal [16] reported GNR-FETs using graded gate engineering. The implemented device shows considerable improvement in SS, voltage gain, and cutoff frequency as compared to normal GNR-FETs [16]. In another implementation, Tamersit [17] observed that in GNR-FETs, short channel parameters can be improved by using the junctionless and multigate technology. The author reported the improvement in SS, DIBL, and threshold voltage roll-off [17]. Radsar et al. [18] reported the performance improvement in GNR-FETs by changing the gate dielectrics with high dielectric coefficient material lanthanum aluminate. The authors observed the improvement in I_{ON}/I_{OFF} ratio, SS, and DIBL as compared to other dielectric materials [18].

Fahad et al. [19] solved analytical models from GNR-TFETs using Schrodinger equations. The designed form channel length is 20 nm. The authors found close agreement of I_{ON}/I_{OFF} ratio and SS with a numerical quantum simulation method [19]. The graphene and SiO_2 oxide interface can also degrade the performance of the device due to the mismatch of structure and tunneling of hot electrons into the oxide [20]. It leads to the degradation of drain current (I_d) and V_{th}. Hence, to improve these parameters, it is proposed that the use of HfO_2 having high-k could be a suitable material as an oxide [21]. For the fabrication of graphene layers on silicon substrates, a rapid CVD system is used. Using this system, a graphene layer having the thickness in 2 to 3 nm can be formed. This represents that the layer of graphene material on the silicon substrate offers the expected mobility for graphene channel FETs. The rapid CVD fabricated the graphene material to be used as channel material, which is equivalent to 1 nm atomic thick layer. With reference to this, in the proposed research work, the graphene material thickness is considered to be 1.5 to 2 nm [22].

3. Design Methodology

The I_d of conventional MOSFETs depends on various parameters. As per Eq. (1), it is observed that I_d is directly proportional to the mobility of electrons (μn) and applied drain-source voltage (V_{ds}) for n-channel MOSFETs. I_d is inversely proportional to the channel length (L). When scaling of MOSFETs is carried out at that time, the channel length is reduced in nanometer size and V_{ds} is also reduced. Due to the reduction in V_{ds}, the overall power consumption of the device reduces, and I_d also degrades. Hence, to improve I_d, the mobility of electrons can be increased, but the mobility of silicon material is limited. To increase the mobility, a new promising material graphene is used in this design, which has a mobility of 30000 cm^2/V.s. Due to the increase in mobility, the performance of the device can be improved.

The short channel parameter SS is directly proportional to depletion capacitance (C_d) and inversely proportional to oxide capacitance (C_{ox}) as per Eq. (2). To improve SS to its ideal value of 60 mV/dec., C_{ox} can be reduced by changing the dielectric material used under the gate terminal. In this design, HfO_2, the dielectric material is used to improve SS. The improvement in SS also improves the I_{ON}/I_{OFF} ratio of the device, which is an essential factor for the digital logic application of the device and low power consumption. DIBL is another short channel effect that depends on V_{ds} and V_{th} as per Eq. (3). DIBL can be controlled by improving V_{th}, which again depends on channel materials and oxide materials. In this research work, the effect of graphene material as a channel is studied, and the simulation results are obtained using the Silvaco TCAD tool. The four designs are discussed in further sections.

$$I_d(lin) = \frac{\mu n.C_{ox}}{2}.\frac{W}{L}.[2(V_{gs} - Vt)V_{ds} - V_{ds}^{\ 2}] \quad (1)$$

$$SS = 60(1 + \frac{C_d}{C_{ox}}) \quad (2)$$

$$DIBL = \frac{V_{th}^{dd} - V_{th}^{low}}{V_{dd}^{high} - V_{dd}^{low}} \quad (3)$$

4. Design of Device Having 100 nm Channel Length

4.1. Design of silicon MOSFET with 100 nm channel length

The silicon channel MOSFET is designed by using the dimensions as per the standard examples from the Silvaco TCAD tool. Fig. 1 shows the designed structure of 100 nm channel length device. The total length of the device in x-direction is 500 nm and the height of the device in y-direction is 65 nm, thus a proper aspect ratio is maintained. The source terminal length in x-direction ranges from 0 nm to 200 nm, and the contact of source ranges from 0 nm to 100 nm, as shown in Fig. 1. The channel region ranges from 200 nm to 300 nm with a height of 15 nm. The drain region ranges from 300 nm to 500 nm, and the drain contact ranges from 400 nm to 500 nm in x-direction. A SiO_2 dielectric material is deposited with 2.5 nm thickness. It ranges from 175 nm to 325 nm over the channel region. A polysilicon contact of 2.5 nm thickness is used to apply gate voltage. The bulk starts from 20 nm to 65 nm in y-direction. The default body voltage is zero.

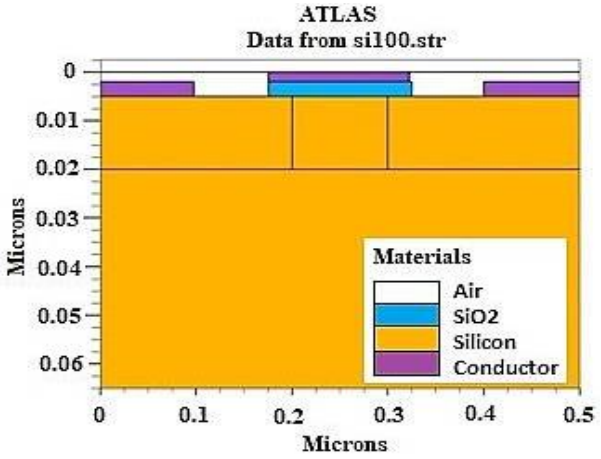

Fig. 1 Silicon channel MOSFET with 100 nm channel length

4.2. Simulation results of 100 nm MOSFET

The designed 100 nm MOSFET is simulated, and various parameters are extracted. Initially, the drain current to gate-source voltage (I_d-V_{gs}) characteristic is plotted. V_{th} is extracted from this plot, the observed value is V_{th} = 0.303V. For DIBL extraction, the device is simulated for two different drain-drain voltage (V_{dd}), i.e., V_{dd}(min) = 0.1 V and V_{dd}(max) = 1 V. The obtained DIBL value is 0.0279 mV/V. The SS value, which decides the speed of the device, is observed to be 79.72 mV/dec (near its ideal value of 60 mV/dec). I_{ON}/I_{OFF} ratio is obtained by finding the values of I_{ON} at V_{dd} = 1 V and I_{OFF} at V_{dd} = 0 V. The ratio observed is $1.73e^{10}$, which is higher enough to switch off the device and for low leakage current. Fig. 2 shows the I_d-V_{gs} characteristics.

Fig. 3 shows the I_d-V_{ds} characteristics to plot and find the saturation slope. The three curves for three different gate voltages are plotted: V_{gs1} = 0.3 V, V_{gs2} = 0.6 V, and V_{gs3} = 1 V. The observed saturation slope value is 2.78e-05. From the characteristics, it is observed that the device offers a very low I_d for V_{gs1} = 0.3 V and V_{gs2} = 0.6 V, and offers sufficient I_d for V_{gs3} = 1 V.

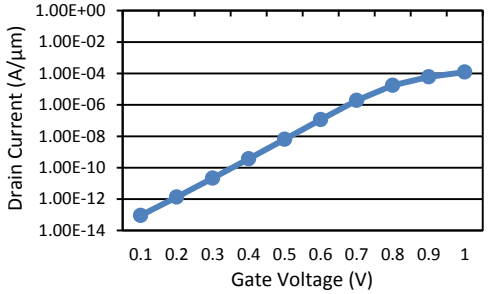

Fig. 2 I_d-V_{gs} characteristics of Si-channel MOSFET (100 nm)

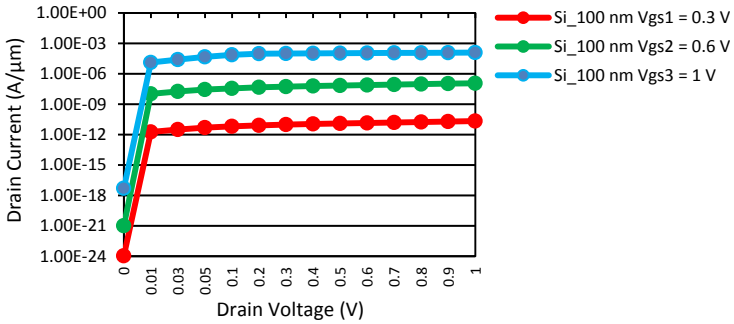

Fig. 3 I_d-V_{ds} with three values of V_{gs} and y-axis with log scale

4.3. Design of graphene FET with 100 nm channel length

The graphene material is not directly available in the Silvaco TCAD tool for simulation purposes. Hence, the design of the graphene channel FET is implemented using the Silvaco TCAD tool by adding graphene as a user-defined material. Graphene is an extract of carbon having very high carrier mobility and a 2-D structure. To implement graphene FET using Silvaco TCAD, one major issue is that graphene needs to be directly available in the tool. Hence, the user needs to define a user-defined material by changing the properties of the existing material. In the Silvaco tool, various materials are available which can be used as an alternative of graphene. One attempt has been reported by Mobarakeh et al. [23]. A 3C-SiC material is used as a graphene channel. Another design using the Silvaco TCAD user-defined material is demonstrated by Kuang et al. [24]. In Silvaco TCAD, three materials have the properties which are close to that of graphene material, as shown in Table 1. In this work, InSb is used as a base material because it has low energy bandgap and higher electron and hole mobility, which is the closest to the properties of graphene material.

Table 1 Different material parameters which are close to graphene material [25]

Material	Eg (eV)	Mun (cm^2/V.s)	Mup (cm^2/V.s)	Nc (per CC)	Nv (per CC)	ni (per CC)	Vsatn (cm/s)	Vsatp (cm/s)
3C-SiC	2.2	1000	50	6.59e+18	1.68e+18	1.1	2.00e+7	1.00e+6
InSb	0.17	78000	750	4.16e+16	6.35e+18	1.92e+16	1.00e+6	1.00e+6
InAs	0.35	33000	460	9.33e+16	8.12e+18	9.99e+14	1.00e+6	1.00e+6

Note: Eg is energy bandgap; Mun is the mobility of electronics; Mup is the mobility of holes; Nc is the effective density of state (conduction band); CC is cubic per centimeter; Nv is the effective density of state in valence band; ni is intrinsic carrier concentration; Vsatn is the saturation velocity of electrons; Vsatp is the saturation velocity of holes.

As per the syntax of user-defined materials, the following statement is included in the code. This statement includes the properties of the user-defined graphene material: "material material = Graphene Eg300 = 0.7 affinity = 4.07 mun = 30000 mup = 30000 Nc300 = 4.16e16 Nv300 = 6.35e18 index.file = graphene.nkuser.group = semiconductor user.default = InSb".

In this statement, a .nk file for graphene material is formed by preparing a table of 499 entries of wavelength and its corresponding refractive index. As demonstrated by Weber [26], the energy bandgap for this simulation is considered 0.7 eV. From these different experiments carried out by Han et al. [27] and Chen et al. [28], it is observed that in GNR, if the ribbon width is reduced below 20 nm, then a sufficient energy bandgap can be achieved, and hence the nanoribbon device can be used as the switching device.

4.4. Defining graphene structure

Fig. 4 shows the original structure of 100 nm silicon MOSFET, which is modified to form the graphene FET. All dimensions are as per the silicon 100 nm design; only the channel material from 200 nm to 300 nm in x-direction and the one from 5 nm to 20 nm in y-direction are replaced with the user-defined graphene material. Fig. 5 shows the I_d-V_{gs} curve by varying the V_{gs} values from 0 V to 1 V with a step of 0.1 V. It has a close agreement with conventional MOSFETs. Fig. 6 shows the family of I_d-V_{ds} curve for three different gate voltages, i.e., V_{gs1} = 0.3 V, V_{gs2} = 0.6 V, and V_{gs3} = 1 V. This curve shows that the graphene FET enters into the saturation region and works like a normal silicon MOSFET.

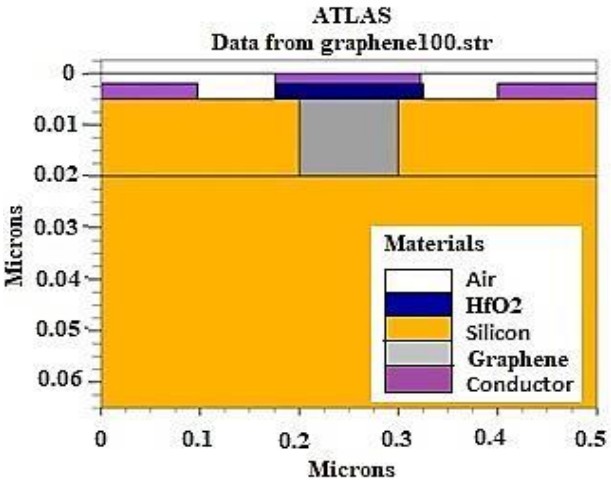

Fig. 4 Structure of 100 nm graphene channel FET

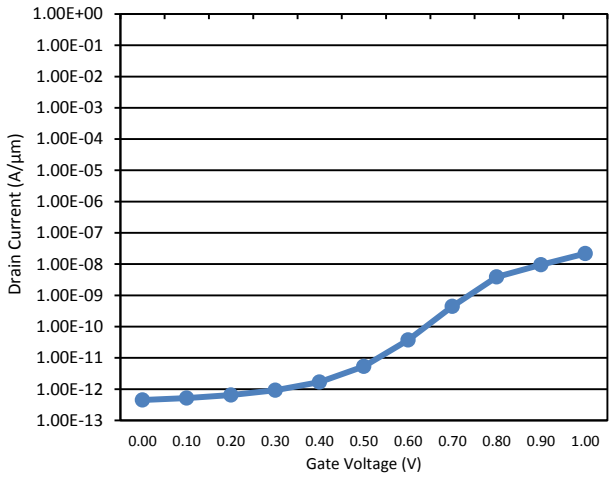

Fig. 5 I_d-V_{gs} curve for 100 nm graphene channel FET

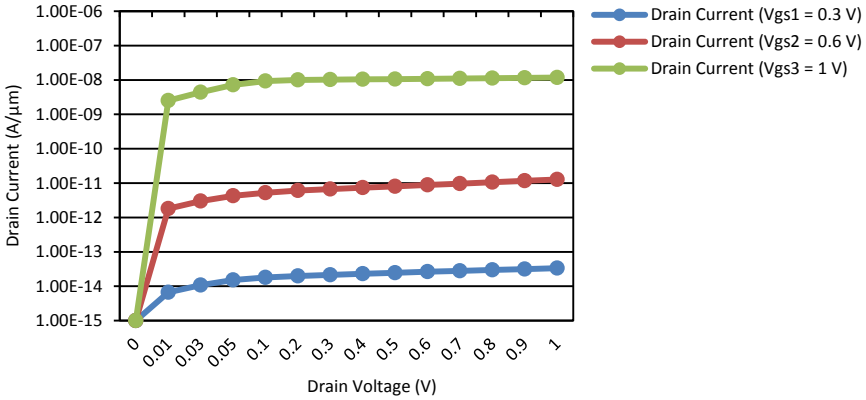

Fig. 6 I_d-V_{ds} characteristics for three gate voltages

5. Design of Device Having 20 nm Channel Length

5.1. Design of graphene FET with 20 nm channel length

The graphene channel MOSFET is designed. As shown in Fig. 7, the original 100 nm device is scaled down to 20 nm device by keeping the aspect ratio. The total length of the device in x-direction is 100 nm and the height of the device in y-direction is 13 nm, thus a proper aspect ratio is maintained. The source terminal length in x-direction ranges from 0 to 40 nm and the contact of the source ranges from 0 to 20 nm. The channel region is formed between 40 nm to 50 nm in x-direction with a height of 20 nm in y-direction. The drain region starts from 60 nm and ends at 100 nm, and the drain contact starts from 80 nm to 100 nm in x-direction. HfO_2 dielectric material is deposited with 2 nm thickness; it ranges from 37.5 nm to 62.5 nm over the channel region. The contact of 2 nm thickness is used to apply gate voltage. The bulk starts from 4 nm to 13nm in y-direction. The default body voltage is zero. Fig. 8 shows I_d-V_{gs} characteristics of the graphene FET for V_{ds} = 0.8 V, and Fig. 9 shows I_d-V_{ds} characteristics for three different gate voltages, i.e., V_{gs1} = 0.3 V, V_{gs2} = 0.6 V, and V_{gs3} = 0.8 V. The device offers more I_d for V_{gs} = 0.8 V.

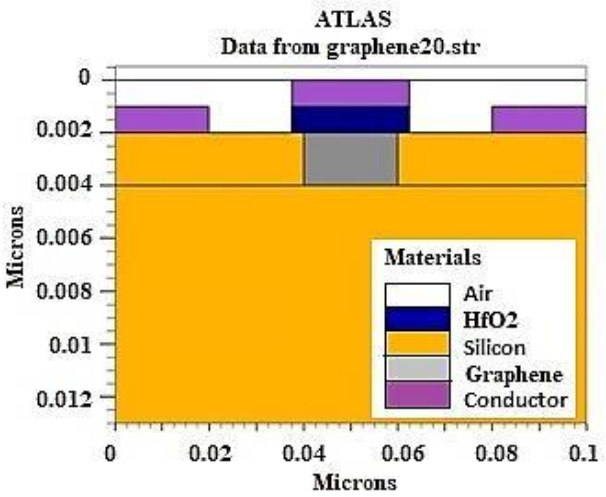

Fig. 7 Structure of 20 nm graphene channel FET

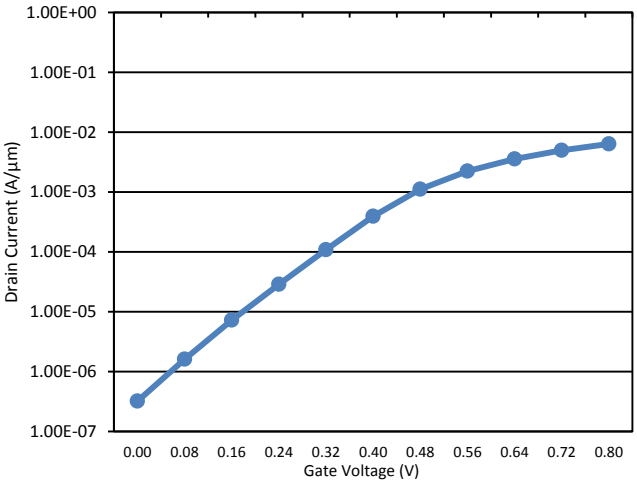

Fig. 8 I_d-V_{gs} curve of 20 nm graphene channel FET

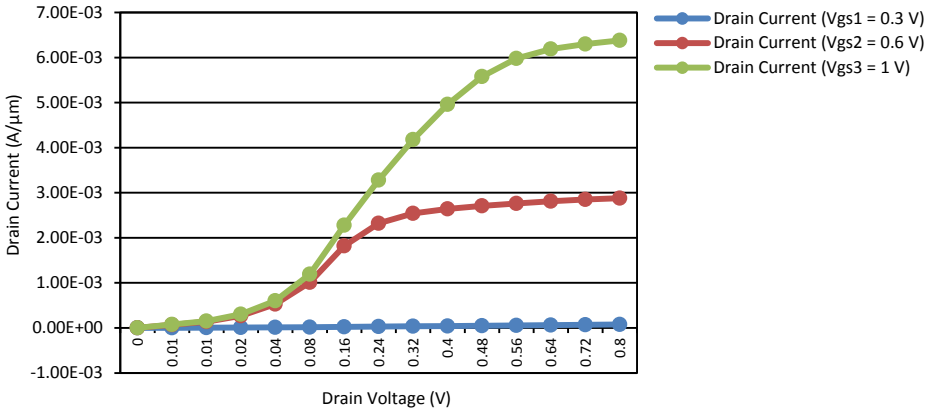

Fig. 9 I_d-V_{ds} curve for three different values of V_{gs}

5.2. Design of 20 nm silicon channel MOSFET

The implementation of a 20 nm silicon channel MOSFET is designed and simulated to compare to the results with the 20 nm graphene channel FET. The structure is shown in Fig. 10. The channel is replaced with silicon material and HfO_2 is used as the dielectric. In the I_d-V_{gs} characteristics for V_{ds} = 0.8V, I_d increases linearly with an increase in V_{gs} after V_{th}. In the I_d-V_{ds} curve for V_{gs1} = 0.3 V, V_{gs2} = 0.6 V, and V_{gs3} = 0.8 V, the small geometry silicon device enters into the saturation region after a pinch-off point. The characteristics of the 20 nm silicon channel MOSFET are embedded with the 20 nm graphene FET design in the result section.

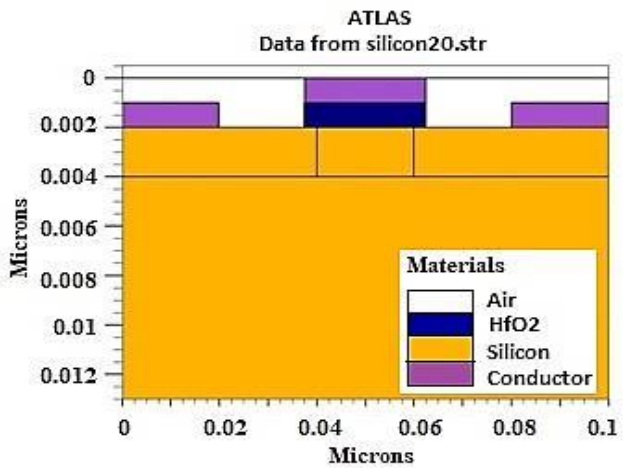

Fig. 10 Structure of 20 nm silicon channel FET

6. Results and Discussion

6.1. Discussion of 100 nm channel length design

The simulation of both the silicon channel and graphene channel FETs is carried out. For the supply voltage of 1 V, it is observed that the graphene FET shows SS = 68.45 mV/dec. and the silicon FET shows SS = 79.6 mV/dec. The SS of graphene FET is close to the ideal value of 60 mV/dec. Hence, it is a suitable candidate for low-power applications. Another short channel parameter DIBL is also reduced to a value of 202 mV/V in the graphene FET as compared to 279 mV/V in the Si-MOSFET, which is better for stable operation of the device. The I_{ON}/I_{OFF} ratio of graphene FET is observed equal to55962, which is still less than that of silicon MOSFET, so it needs to be improved further. The I_d(max) of silicon MOSFET is more than that of graphene FET. Table 2 shows a comparison of all parameters.

In the graphene FET design, by changing gate dielectric material from SiO_2 to HfO_2, the improvement in parameters is observed. Fig. 11 shows overlay characteristics of both FETs. From the characteristics, it is observed that the Si-MOSFET offers more current for different gate voltages; hence, further scaling of these two devices is carried out and a 20 nm FET is designed to observe and improve short channel effects. From Table 2, it is observed that graphene material can be used as a channel material to replace silicon because the behavior of the graphene FET is found to be identical to conventional MOSFETs. The I_d of silicon FET is more than that of graphene FET due to the large channel length and sufficient bandgap of silicon material.

The SS in graphene FET for HfO_2 dielectric material is observed to be 68.45 mV/decade. It is due to an increase in C_{ox}, which depends on dielectric material and oxide thickness (t_{ox}). As the dielectric constant of HfO_2 is high and t_{ox} is only 2.5 nm which is low, the C_{ox} value increases. As per Eq. (2), SS depends on C_{ox}. The SS decreases due to an increase in the C_{ox} value. This decrease in SS is close to the ideal value of SS. The I_{ON}/I_{OFF} ratio is still more in the silicon FET due to the high I_{ON} caused by the sufficient bandgap available in silicon material. The DIBL is reduced in the graphene FET due to more control of gate voltage on channel carriers because of better conductivity of graphene material and high-k gate dielectric material.

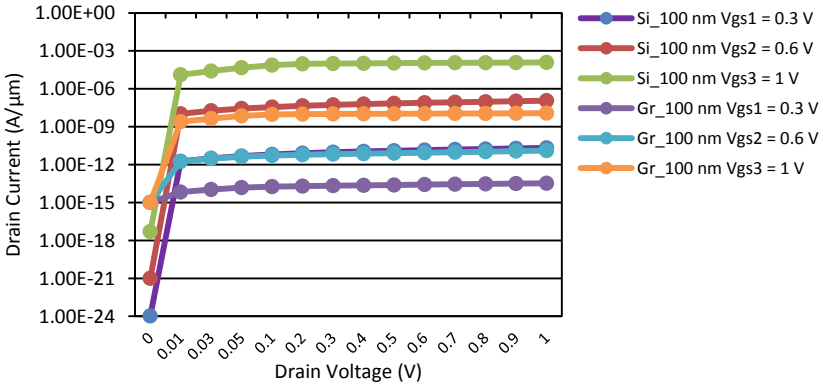

Fig. 11 Overlay characteristics of 100 nm Si-MOSFET and graphene FET

Table 2 Comparison of silicon and graphene channel MOSFETs at 100 nm gate length

Device/parameter	Si-MOSFET	Graphene FET (with SiO_2)	Graphene FET (with HfO_2)
Channel length (nm)	100	100	100
V_{dd}(max) (V)	1	1	1
Electron mobility (cm^2/V.s)	1000	30000	30000
Hole mobility (cm^2/V.s)	500	30000	30000
Bandgap (eV)	1.08	0.7	0.7
Channel material	Silicon	Graphene	Graphene
Gate dielectric material	SiO_2	SiO_2	HfO_2
V_{th} (V)	0.303	0.322	0.357
Subthreshold swing (mV/dec)	79.6	93.0	68.45
I_d(max) (A/µm)	0.000122	2.18e-08	1.69e-6
I_{ON}/I_{OFF}	1.73e10	984.21	55962.56
DIBL (mV/V)	279	202	202

6.2. Discussion of 20 nm channel length design

The implemented graphene channel FET and silicon channel FET at 20 nm channel length are compared as shown in Table 3. It is observed that the graphene FET offers V_{th} = 0.040 V, and silicon MOSFET offers V_{th} = 0.021 V. The observed SS is 114 mV/dec in the graphene FET and 115 mV/dec in the silicon MOSFET. These values need further improvement. The I_d value is more in the graphene FET for V_{ds} = 0.8 V, as compared to the silicon MOSFET. The observed I_{ON}/I_{OFF} ratio is 14379, which shows the improvement in the graphene FET, so it is suitable for low power applications. The observed DIBL in the graphene FET is 123 mV/V, which is less than that of the silicon channel MOSFET. The current work is also compared with the already published work, and it can be seen that the graphene FET shows the improvement in I_d(max) due to the high mobility of graphene material and DIBL parameters.

Fig. 12 shows the comparison curve of I_d-V_{gs} for V_{ds} = 0.8 V. It is observed that the graphene FET offers a high I_d value for the same voltage of V_{ds} as compared to the silicon MOSFET. Fig. 13 shows the combined curve of I_d-V_{ds} for three different gate voltages. The comparison shows that the graphene FET offers more I_d than the silicon MOSFET, which is a benefit for the high-speed operation of the device. As per Table 3, the I_d(max) is the highest as compared to others due to the excellent electrical conductivity of graphene material and higher mobility. However, due to this, there is an increase in SS, which is still lower than that of the silicon FET. The I_d of the silicon FET decreases due to short channel effects. The I_{ON}/I_{OFF} ratio of the graphene FET increases due to the low leakage in graphene material in "off" conditions. The high value of I_{ON} also contributes to the increase of this ratio. The DIBL parameter of the graphene FET is also lower than that of the Si-MOSFET due to the better control of gate voltage on the channel in the short device. The I_d of the graphene FET is the highest among all published results shown in Table 3 due to the higher mobility of graphene material. SS, DIBL, and I_{ON}/I_{OFF} ratio needs to be further improved for low power applications.

Table 3 Comparison of the parameters in graphene and silicon MOSFETs

Device	Si-MOSFET (this work)	Graphene FET (this work)	SOI-JLT [11]	FinFET [12]	GNR-TFET [19]
Channel length (nm)	20	20	10	8	20
V_{dd}(max) (V)	0.8	0.8	0.8	0.9	0.1
Electron mobility (cm^2/V.s)	1000	30000	1000	1000	Not mentioned
Hole mobility (cm^2/V.s)	500	30000	500	500	Not mentioned
Bandgap (eV)	1.08	0.7	1.08	1.08	0.289
Base material	Silicon	User-defined graphene	Silicon	Silicon	Graphene
Gate dielectric material	HfO_2	HfO_2	HfO_2	SiO_2	SiO_2
V_{th} (V)	0.0218	0.040	0.327	-	-
Subthreshold swing (mV/dec.)	115	114	109.9	63.13	27.4
I_d(max) (A/µm)	0.0027	0.00638	330×10^{-6}	0.00001	4.4×10^{-6}
I_{ON}/I_{OFF}	6401	14379	420000	10^6	116
DIBL (mV/V)	129	123	218	85	-

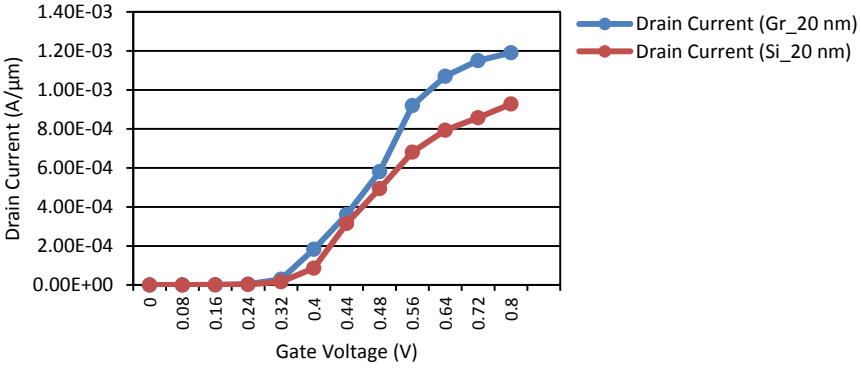

Fig. 12 Comparison curve of I_d-V_{gs} for V_{ds} = 0.8 V

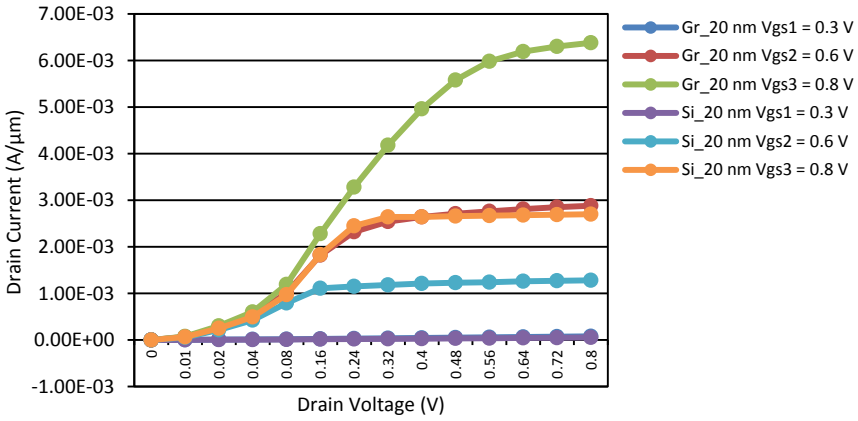

Fig. 13 Combined curve of I_d-V_{ds} for three different gate voltages

7. Conclusions

The Silvaco TCAD tool does not have an inbuilt graphene material; hence, a user-defined graphene material is added in this study. This material is formed by using the parameters of the existing materials, which are close to that of graphene, and the simulation is carried out. The first graphene channel FET with 100 nm channel length is implemented using HfO_2 material as the dielectric under gate terminal, and compared with another implementation of 100 nm silicon channel FET. The results are in good agreement with each other. The high dielectric material HfO_2 offers less leakage current; hence, it improves the I_{ON}/I_{OFF} ratio of the device. The graphene FET has improved SS and DIBL parameters. To study the short channel effects, further scaling of the graphene FET is carried out to the 20 nm channel length. This small channel device also shows the improvement in DIBL, SS, and I_d(max) over the 20 nm silicon FET and other published results. The saturation curves of the both are plotted and compared, and it is observed that the graphene FET provides more I_d as compared to the silicon MOSFET. As a high I_{ON}/I_{OFF} ratio is observed, it is concluded that the graphene channel FET can be a perfect replacement for a conventional silicon MOSFET at a small channel length for low power and high-speed applications. Further improvement of the implemented FET using the user-defined graphene material could be achieved by using a double gate structure.

Conflicts of Interest

The authors declare no conflict of interest.

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