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DV-EXCCCII Based Resistor-Less Current-Mode Universal Biquadratic Filter

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Abstract

This study aims to present a new resistor-less current-mode multi-input single-output universal filter. The current-mode's design approach is used to obtain the proposed circuit. This circuit employs a single differential voltage extra-X current controlled current conveyor (DV-EXCCCII) and two grounded capacitors. This multifunction filter circuit offers low-pass, high-pass, all-pass, band-pass, and band-reject filters at a single output terminal without passive component matching constraints. The same circuit topology can obtain all second-order filter functions with different input conditions. The proposed circuit design is electronically adjustable with the bias current of DV-EXCCCII. Because of its high output impedance, this arrangement is suitable for cascading other current-mode circuits. The proposed circuit is simulated by Cadence Spectre with 0.18 μm UMC CMOS technology process parameters at ± 0.9 V supply voltages. The simulation results agree well with the theoretical concept of the proposed circuit.

Keywords: biquad filter, DV-EXCCCII, electronically tunable, analog building block, current-mode filter

1. Introduction

Analog filters are essential building blocks in several applications such as communication systems, analog signal processing, instrumentation systems, control engineering, signal generator, etc. Analog filters eliminate undesired signals from the desired ones by allowing signals to pass at specific frequencies. Analog filters may operate in multiple modes in integrated circuits, such as voltage, current, trans-admittance, and trans-impedance [1]. Recently, there has been a growing trend in designing circuits using current-mode (CM) blocks. These circuits have numerous beneficial features, such as a high slew rate, higher linearity, good frequency performance, higher dynamic range, simple circuit design, and low voltage operation. Over the period, several current-mode active blocks evolved [2-24]. Some of the most important active blocks in the literature are CCII [2], CCCII [3-4], DVCC [5-6], OFCC [7-8], CDTA [9], MOCCII [10-11], VDTA [12], ICCII [13], CFTA [15], VDCC [16], ZC-CFTA [17], DOCCII [18], MOCCA [19], MO-CCCA [20], CCCCTA [21], DDCC [22], EX-CCCII [23], DV-EXCCCII [24], LT1228 [25], FTFNTA [26], DXCCTA [27], FDCCII [14, 28], and many more.

Various current-mode and voltage-mode filters using these active elements are available in the open literature. The CM filters employing DVCC are presented in [5-6]. The filter shown in [5] uses two DVCCs, one floating, and four grounded passive components, whereas the filter proposed in [6] employs three DVCCs and five grounded passive components. The use of more passive components increases circuit complexity. The electronically tunable filters with three OFCCs and more passive elements are presented in [7-8]. Two CDTAs and one current amplifier-based electronically tunable filter are presented

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in [9]. This filter has high output impedance and uses two grounded capacitors. The filters employing three multi-output CCIIs are given in [10-11]. These filters are not electronically tunable. Filters based on a single active element are described in [12, 14, 16, 22], whereas filters described in [13, 15, 17-21] use more analog blocks.

An electronically tunable active element with an extra input current terminal is proposed later, and its first-order filter application is represented in [23]. A novel electronically tunable analog block with a differential input stage and an extra input current terminal is proposed in [24]. This active element has a wide application because it exhibits the properties of both DVCC and EX-CCCII. A filter proposed in [24] uses a single DV-EXCCCII and is electronically tunable. The voltage-mode filter presented in [25] employs two LT1228s, four resistors, and two capacitors. The use of more passive elements increases the area of the circuit. Due to the reduction in the supply voltages, low voltage headroom is available in modern integration technologies. So, the voltage-mode filters suffer from low dynamic range and output swing limitation. Therefore, the current-mode filters are preferred over the voltage-mode filters.

This study describes a novel CM filter design which employs one DV-EXCCCII and two capacitors. The proposed structure is resistor-less, and the capacitors employed in this structure are grounded, so it is preferable for IC implementation. Due to its high output impedance, the proposed circuit can cascade the other current mode circuits. Due to the bias current of DV-EXCCCII, the proposed filter is electronically tunable. Furthermore, the proposed filter does not need passive components matching conditions for the filter realization. The proposed structure can achieve all fundamental functions of a second-order filter, i.e., a low-pass filter (LPF), a high-pass filter (HPF), an all-pass filter (APF), a band-pass filter (BPF), and a band-reject filter (BRF). Although the proposed circuit can also be designed using EX-CCCII, this study focuses on a filter circuit with a more generalized active element. As a result, a filter circuit is proposed using DV-EXCCCII.

The remnant of this study is structured as follows: Section 2 presents the basic concept of DV-EXCCCII. Section 3 shows a detailed analysis of the proposed filter structure. This section also investigates the non-ideal effect of DV-EXCCCII on the proposed circuit. Section 4 compares the derived filter with previously available CM filters, whereas Section 5 provides the simulation results. Section 6 presents the practical implementation of DV-EXCCCII, while Section 7 presents various conclusion remarks.

2. Basic Concept of DV-EXCCCII

The DV-EXCCCII [24] combines the merits of DVCC and EX-CCCII which is already reported in the literature. The DVCC is a modified version of the current conveyor with a differential input stage. At the same time, the EXCCCII is a variant of the current-controlled current conveyor with an extra-X terminal. The DV-EXCCCII uses these two analog blocks with a differential input stage and an extra current terminal. The DV-EXCCCII is an analog building block that can implement various current-mode and voltage-mode circuits.

Fig. 1 shows the symbol of DV-EXCCCII, and Fig. 2 shows its internal CMOS representation. The relationship between the input and output terminal of DV-EXCCCII is given by the matrix below,

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_{X1} & 0 & 0 & 0 \\ 1 & -1 & 0 & R_{X2} & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{1}$$

The RX1 and RX2 are internal resistances at input terminals X1 and X2, respectively. The value of these internal resistances is,

$$R_{X1} = R_{X2} = R_X = \frac{1}{\sqrt{8\mu C_{0X}(\frac{W}{L})I_o}} \tag{2}$$

Here μ is the mobility, C_{ox} is oxide capacitance, W/L is the aspect ratio, and I_0 is the bias current of an active block. The internal resistances R_{X1} and R_{X2} are used instead of external resistance, making the overall circuit implementation suitable for IC implementation. We can notice from the above expression that if the aspect ratios of transistors M2 and M3 are the same and M5 and M6 are the same, then intrinsic resistance at both current terminals will also be equal. Transistors M21, M22, M23, and M24 generate a differential voltage (V_{Y1}–V_{Y2}) at the input current terminal (X1, X2). All Z terminals used here are high output impedance terminals. This current-mode block has internal bias current I_0, due to which DV-EXCCCII offers electronic tunability. The positive sign of the Z terminal indicates that the currents flowing through terminal X and terminal Z are in the same phase. However, a negative symbol means that the current through the Z terminal is out of phase from the current flowing through the X terminal.

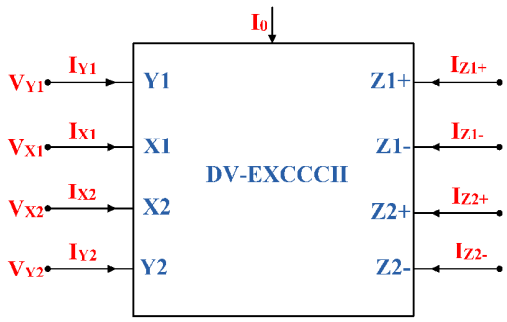


Fig. 1 Symbolic representation of DV-EXCCCII

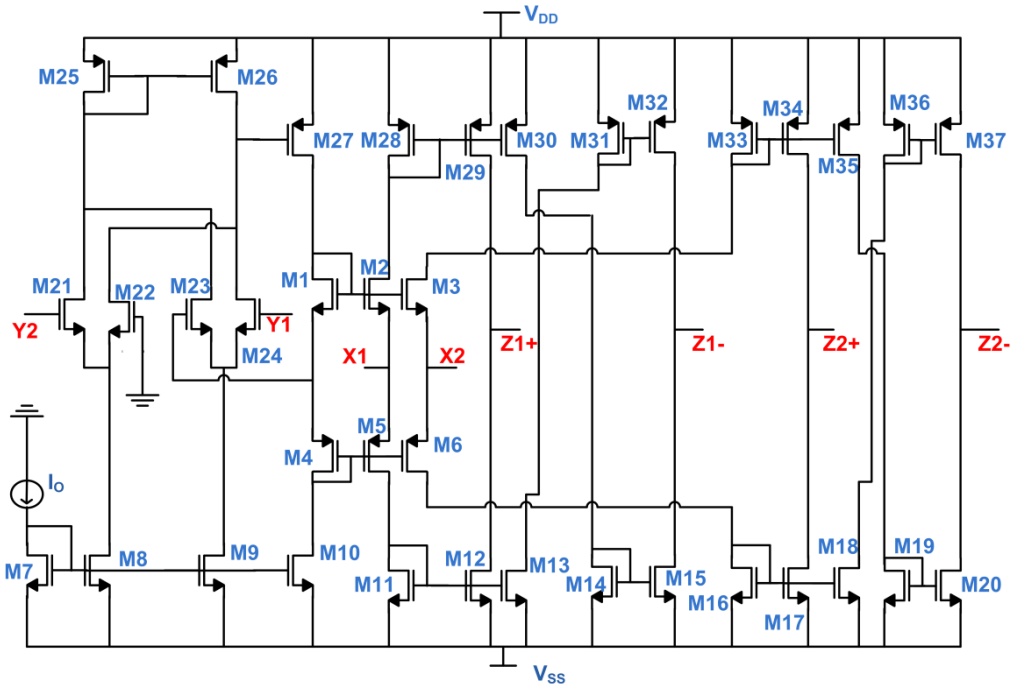


Fig. 2 Internal structure of DV-EXCCCII [26]

3. Proposed Universal Filter

3.1. Circuit analysis

A single DV-EXCCCII based proposed filter, displayed in Fig. 3, can produce all five fundamental filters utilizing appropriate input combinations. This circuit can give the output current as,

$$I_{out} = \frac{I_3(1+R_{X2}C_1s+R_{X1}R_{X2}C_1C_2s^2)-I_2R_{X1}C_1s+I_1}{1+R_{X2}C_1s+R_{X1}R_{X2}C_1C_2s^2} \tag{3}$$

The intrinsic resistance at terminals X1 and X2 can be equal by matching the transistors M2, M3, M5, and M6, i.e., $R_{X1} = R_{X2} = R_X$. The proposed circuit uses the following input combinations:

(1) For LPF, response, $I_2 = I_3 = 0$ and $I_1 = I_{in}$ are taken.

(2) For HPF, $I_2 = I_3 = I_{in}$ and $I_1 = -I_{in}$ are taken.

(3) For APF, $I_2 = 2I_{in}$, $I_1 = 0$, and $I_3 = I_{in}$ are chosen.

(4) For BPF, $I_2 = I_{in}$ and $I_1 = I_3 = 0$ are chosen.

(5) For BRF, $I_2 = I_3 = I_{in}$ and $I_1 = 0$ are taken.

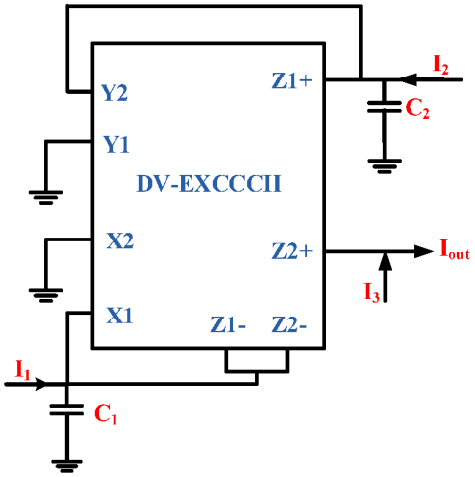


Fig. 3 Proposed biquadratic filter configuration

The characteristic equation (D(s)) of the proposed circuit is,

$$D(s) = R_{X1}R_{X2}C_1C_2s^2 + R_{X2}C_1s + 1 \tag{4}$$

The angular frequency (ω_0), bandwidth (BW), and quality factor (Q) of the proposed filter are,

$$\omega_0 = \frac{1}{\sqrt{R_{X1}R_{X2}C_1C_2}} \tag{5}$$

$$BW = \frac{1}{R_{X1}C_2} \tag{6}$$

$$Q = \sqrt{\frac{R_{X1}C_2}{R_{X2}C_1}} \tag{7}$$

Taking $R_{X1} = R_{X2} = R_X$, it yields

$$\omega_0 = \frac{1}{R_X\sqrt{C_1C_2}} \tag{8}$$

$$BW = \frac{1}{R_XC_2} \tag{9}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{10}$$

Eqs. (8)-(10) show that ω_0 depends on the bias current, so the pole frequency can be adjusted by tuning I_0. Whereas Q does not depend on I_0, the change in the bias current would not affect the value of Q. Therefore, ω_0 and Q can be modified independently. The sensitivities due to passive components and intrinsic resistances are evaluated and given as,

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_{X1}}^{\omega_0} = S_{R_{X2}}^{\omega_0} = -\frac{1}{2} \tag{11}$$

$$S_{R_{X1}}^{Q} = S_{C_2}^{Q} = -S_{R_{X2}}^{Q} = -S_{C_1}^{Q} = \frac{1}{2} \tag{12}$$

$$S_{R_{X1}}^{BW} = S_{C_2}^{BW} = -1; S_{R_{X2}}^{BW} = S_{C_1}^{BW} = 0 \tag{13}$$

Eqs. (11)-(13) show that the sensitivities due to passive components and internal resistances are low.

3.2. Non-ideal DV-EXCCCII

This section shows the influence of current and voltage gain errors in the response of the reported filter circuit. Considering non-ideal DV-EXCCCII, its port relationship is,

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_{11} & -\beta_{12} & R_{X1} & 0 & 0 & 0 \\ \beta_{21} & -\beta_{22} & 0 & R_{X2} & 0 & 0 \\ 0 & 0 & \pm\alpha_{1\pm} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm\alpha_{2\pm} & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{14}$$

Here, β_{11} and β_{12} are non-ideal voltage transfer gain coefficients from terminals Y1 and Y2 to X1, respectively. Similarly, β_{21} and β_{22} are voltage transfer gain coefficients from Y1 and Y2 to the X2 terminal. Whereas α_{1+} and α_{1-} are non-ideal current transfer gain coefficients from X1 to Z1+ and Z1- terminals. Similarly, α_{2+} and α_{2-} are coefficients from X2 to Z2+ and Z2- terminals, respectively.

As explained earlier, all α coefficients are non-ideal current gain between Z and X terminals, whereas all β coefficients are non-ideal voltage gain between X and Y terminals. The value of α and β [29] are,

$$\alpha(s) = \frac{\alpha_0}{1+\tau_\alpha s} \tag{15}$$

$$\beta(s) = \frac{\beta_0}{1+\tau_\beta s} \tag{16}$$

where $\tau_\beta = \frac{1}{\omega_\beta}$ and $\tau_\alpha = \frac{1}{\omega_\alpha}$. Here ω_α and ω_β are angular pole frequencies. The DC voltage gain β_0 and current gain α_0 are ideal unity, the voltage tracking error ε_β and current tracking error ε_α, as shown below, define the DC voltage and current gain.

$$\beta_0 = 1+\varepsilon_\beta \tag{17}$$

$$\alpha_0 = 1+\varepsilon_\alpha \tag{18}$$

These tracking errors are, $|\varepsilon_\beta| \ll 1$, $|\varepsilon_\alpha| \ll 1$.

Considering non-idealities of DV-EXCCCII, the output current is,

$$I_{out} = \frac{p(s)I_3 - q(s)I_2 + rI_1}{p(s)} \tag{19}$$

where

$$p(s) = R_{X1}R_{X2}C_1C_2s^2 + \beta_{12}\alpha_{1+}R_{X2}C_1s + (1-\alpha_{1-})R_{X2}C_2s + \beta_{22}\alpha_{2-}\alpha_{1+} \tag{20}$$

$$q(s) = \beta_{22}(R_{X1}C_1s + 1 - \alpha_{1-}) \tag{21}$$

$$r = \alpha_{1+}\beta_{22} \tag{22}$$

The parameters, ω_0, BW, and Q are as follows,

$$\omega_0 = \sqrt{\frac{\beta_{22}\alpha_{2-}\alpha_{1+}}{R_{X1}R_{X2}C_1C_2}} \tag{23}$$

$$BW = \frac{\beta_{12}\alpha_{1+}C_1 + (1-\alpha_{1-})C_2}{R_{X1}C_1C_2} \tag{24}$$

$$Q = \frac{1\sqrt{C_1C_2\beta_{22}\alpha_{2-}\alpha_{1+}}}{C_1\beta_{12}\alpha_{1+} + C_2(1-\alpha_{1-})} \tag{25}$$

Eqs. (23)-(25) show that the non-ideal DV-EXCCCII slightly modifies the values of these parameters. Considering non-ideal DV-EXCCCII, the sensitivities of pole frequency are,

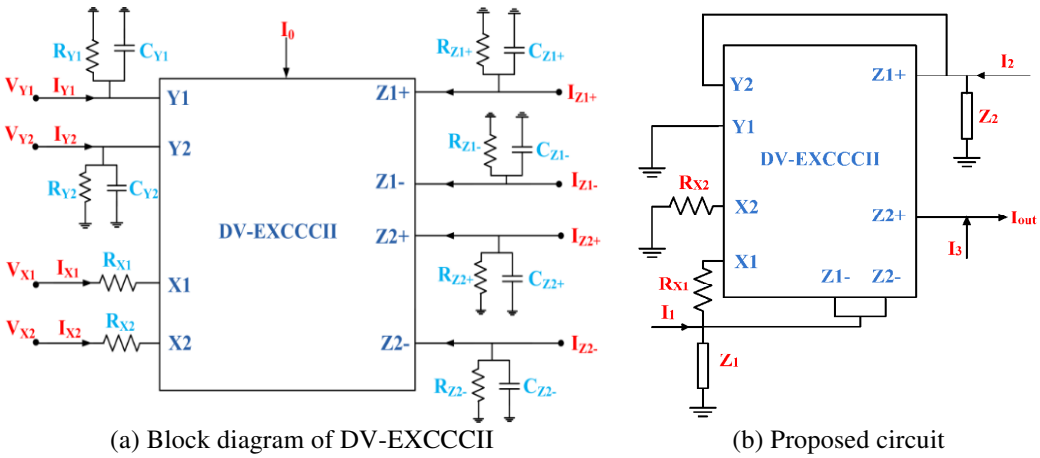
$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_{X1}}^{\omega_0} = S_{R_{X2}}^{\omega_0} = -\frac{1}{2} \tag{26}$$

$$S_{\beta_{22}}^{\omega_0} = S_{\alpha_{2-}}^{\omega_0} = S_{\alpha_{1+}}^{\omega_0} = \frac{1}{2} \tag{27}$$

$$S_{\beta_{11}}^{\omega_0} = S_{\beta_{12}}^{\omega_0} = S_{\beta_{21}}^{\omega_0} = S_{\alpha_{2+}}^{\omega_0} = S_{\alpha_{1-}}^{\omega_0} = 0 \tag{28}$$

Eqs. (26)-(28) show that the sensitivities of the pole frequency considering non-idealities are below unity.

3.3. Parasitic effect



(a) Block diagram of DV-EXCCCII (b) Proposed circuit

Fig. 4 Circuit under the parasitic influence

Fig. 4(a) shows the symbol of DV-EXCCCII with its parasitic components. R_{X1} and R_{X2} are low-value parasitic resistances at ports X1 and X2. The parasites $R_{Y1}//C_{Y1}$ and $R_{Y2}//C_{Y2}$ appear at ports Y1 and Y2, respectively. Furthermore, parasites $R_{Z1+}//C_{Z1+}$ and $R_{Z1-}//C_{Z1-}$ appear at ports Z1+ and Z1-, respectively, while $R_{Z2+}//C_{Z2+}$ and $R_{Z2-}//C_{Z2-}$ are parasites that appear at terminals Z2+ and Z2-, respectively. The values of R_{Y1}, R_{Y2}, $R_{Z1\pm}$, and $R_{Z2\pm}$ are high, and that of C_{Y1}, C_{Y2}, $C_{Z1\pm}$, and $C_{Z2\pm}$ are low. Fig. 4(b) illustrates the proposed filter architecture when parasitic elements are present. Some assumptions are taken into account to avoid mathematical complexity, and they are as follows:

$$R_{eq1} = R_{Z1-} // R_{Z2-} \tag{29}$$

$$C_{eq1} = C_1 + C_{Z1-} + C_{Z2-} \tag{30}$$

$$R_{eq2} = R_{Y2} // R_{Z1+} \tag{31}$$

$$C_{eq2} = C_2 + C_{Y2} + C_{Z1+} \tag{32}$$

$$Z_1 = \frac{R_{eq1}}{1 + sR_{eq1}C_{eq1}} \tag{33}$$

$$Z_2 = \frac{R_{eq2}}{1 + sR_{eq2}C_{eq2}} \tag{34}$$

By considering the parasitic impedances of DV-EXCCCII, the output of the proposed circuit is,

$$I_{out} = \frac{AI_1 - B(s)I_2 + I_3 D(s)}{D(s)} \tag{35}$$

where,

$$A = R_{eq1}R_{eq2} \tag{36}$$

$$B(s) = R_{X1}R_{eq2}(1 + sR_{eq1}C_{eq1}) \tag{37}$$

$$D(s) = as^2 + bs + c \tag{38}$$

here,

$$a = R_{X1}R_{X2}R_{eq1}R_{eq2}C_{eq1}C_{eq2} \tag{39}$$

$$b = R_{X2}R_{eq1}R_{eq2}C_{eq1} + R_{X1}R_{X2}R_{eq1}C_{eq1} + R_{X1}R_{X2}R_{eq2}C_{eq2} \tag{40}$$

$$c = R_{X1}R_{X2} + R_{eq1}R_{eq2} + R_{X2}R_{eq2} \tag{41}$$

The parameters ω_0, BW, and Q of the filter under the influence of parasitic elements of DV-EXCCCII are,

$$\omega_0 = \sqrt{\frac{R_{X1}R_{X2} + R_{eq1}R_{eq2} + R_{X2}R_{eq2}}{R_{X1}R_{X2}R_{eq2}C_{eq1}C_{eq2}}} \tag{42}$$

$$BW = \frac{R_{eq1}R_{eq2}C_{eq1} + R_{X1}R_{eq1}C_{eq1} + R_{X1}R_{eq2}C_{eq2}}{R_{X1}R_{eq1}R_{eq2}C_{eq1}C_{eq2}} \tag{43}$$

$$Q = \sqrt{\frac{R_{X1}R_{X2}R_{eq1}R_{eq2}C_{eq1}C_{eq2}(R_{X1}R_{X2}+R_{eq1}R_{eq2}+R_{X2}R_{eq2})}{R_{X1}R_{X2}R_{eq1}C_{eq1}+R_{X1}R_{X2}R_{eq2}C_{eq2}+R_{X2}R_{eq1}R_{eq2}C_{eq1}}} \tag{44}$$

The values of R_{eq1} and R_{eq2} are very high, hence Eqs. (42)-(44) are reduced as follows:

$$\omega_0 = \frac{1}{\sqrt{R_{X1}R_{X2}C_{eq1}C_{eq2}}} \tag{45}$$

$$BW = \frac{1}{R_{X1}C_{eq2}} \tag{46}$$

$$Q = \sqrt{\frac{R_{X1}C_{eq2}}{R_{X2}C_{eq1}}} \tag{47}$$

Eqs. (45)-(47) show that the filter parameters depend on the parasitic capacitances that are low in value. Therefore, these parameters do not deviate much from the theoretical values. Hence the performance of the filter is slightly affected by parasitic elements.

4. Comparative Study

Table 1 shows the comparison of the proposed circuit with the previously available biquadratic filters. A single active element and minimum passive components-based filter configurations are noteworthy. The use of more active and passive components increases chip area and, as a result, circuit complexity. The filter circuits given in [3-11, 13, 15, 17-21] employ more active elements. Some filter circuits [3-8, 10-14, 16, 18, 20-21] use many passive components. Furthermore, the grounded passive components-based structures are easy for IC implementation. The filters reported in [5, 11, 22] employ floating passive components.

The realization of all fundamental filter responses of the biquadratic filter without passive component matching conditions is of great importance. It becomes easy to realize the filter functions that are not interrupted by component values. The value of the quality factor, bandwidth, and pole frequency will be affected by the matching condition applied to achieve filter responses and cannot be tuned arbitrarily. Some filters [4-5, 16, 21-22] require matching constraints to realize the filter response. The filter circuit configurations with high output impedance can cascade other circuits. Filters reported in [12, 16, 22] do not have high output impedance terminals. The filter parameters are usually a function of aging, temperature, and other environmental conditions, so a circuit having electronic tuning properties is preferred. However, several reported filters [10-14, 18, 22] are not electronically tunable.

The proposed circuit can obtain all the fundamental second-order filters at a single terminal without any passive component matching constraints. This filter employs a single DV-EXCCCII and two grounded capacitors. Moreover, the proposed filter has high output impedance terminal, and it is also electronically tunable.

5. Simulation Results

The reported DV-EXCCCII based current-mode filter is verified using CADENCE VIRTUOSO SPECTRE simulator in 0.18 µm UMC CMOS technology. The DC power supply voltages $V_{DD} = -V_{SS} = 0.9$ V are used for simulations. Table 2 shows the aspect ratio of all MOS transistors used. The capacitor values are taken as $C_1 = C_2 = 50$ pF in all the simulations. The bias current $I_0 = 100$ µA is taken to get $R_{X1} = R_{X2} = 813$ Ω. As a result, the pole frequency and quality factors are 3.9 MHz and 1, respectively.

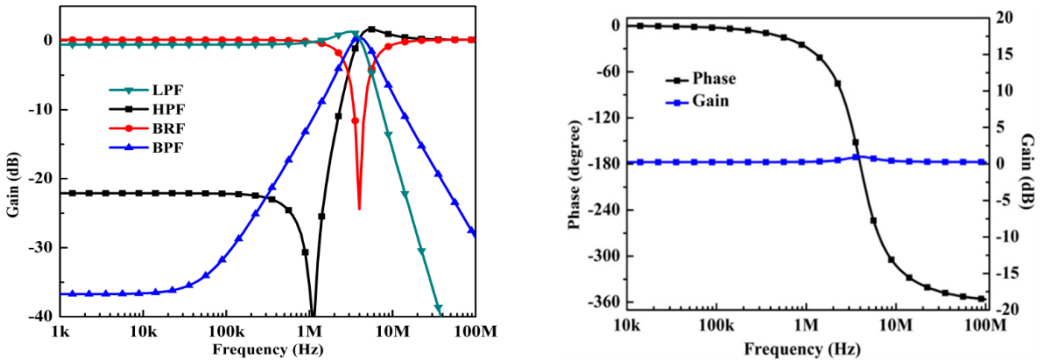
Table 1 Comparative study

Reference	ABB Type	No. of ABBs	Number of resistors		Number of capacitors		High output impedance	Tunability	Technology	Power supplies (V)	Matching required	Universal	Power consumption (mW)	THD (%)	Frequency (f_0)	Area
			Floating	Grounded	Floating	Grounded										
[3]	CCCII	5	0	0	0	3	Yes	Yes	BJT	± 2.5	No	Yes	---	---	318.3 kHz	---
[4]	CCCII	5	0	0	0	3	Yes	Yes	0.13 µm	± 0.75	Yes	Yes	5.48	> 6	33.86 kHz	---
[5]	DVCC	2	1	2	0	2	Yes	Yes	0.13 µm	± 0.75	Yes	Yes	0.81	> 4	3.18 MHz	---
[6]	DVCC	3	0	3	0	2	Yes	Yes	0.18 µm	± 0.9	No	Yes	0.462	> 5	3.18 MHz	0.0208 mm2
[7]	OFCC	3	0	3	0	2	Yes	Yes	0.5 µm	± 1.5	No	Yes	---	---	320 kHz	---
[8]	OFCC	3	0	2	0	2	Yes	Yes	0.5 µm	± 1.5	No	Yes	---	---	1.59 MHz	---
[9]	CDTA, CA	2, 1	0	0	0	2	Yes	Yes	0.18 µm	± 0.9	No	No	1.15	> 7	1 MHz	---
[10]	MOCCII	3	0	3	0	2	Yes	No	0.35 µm	± 1.65	No	Yes	---	---	198.9 kHz	---
[11]	MOCCII	3	2	3	0	2	Yes	No	0.18 µm	± 1.25	No	Yes	---	---	281.35 kHz	---
[12]	VDTA	1	0	1	0	2	No	No	0.18 µm	± 1	No	Yes	---	---	---	---
[13]	ICCII	3	0	4	0	2	Yes	No	0.18 µm	± 0.8	No	Yes	0.674	1.12	159 MHz	---
[14]	FDCCII	1	0	2	0	2	Yes	No	0.35 µm	± 1.3	No	Yes	---	3	1.59 MHz	---
[15]	CFTA	4	0	0	0	2	Yes	Yes	BJT	± 3	No	Yes	---	1.8	153 kHz	---
[16]	VDCC	1	0	2	0	2	No	Yes	0.18 µm	± 0.9	Yes	Yes	0.72	2.48	8.9 MHz	---
[17]	ZC-CFTA	4	0	0	0	2	Yes	Yes	BJT	± 3	No	Yes	12.2	3	159 kHz	---
[18]	DOCCII, DOCCIII	2, 1	0	2	0	2	Yes	No	0.5 µm	± 2.5	No	Yes	---	---	34 kHz	---
[19]	CCCII, MOCCA	2, 1	0	0	0	2	Yes	Yes	0.5 µm	± 1.5	No	Yes	---	---	39 kHz	---
[20]	DOCCII, MO-CCCA	2, 1	0	2	0	2	Yes	Yes	0.35 µm	± 1.5	No	Yes	---	6	1 MHz	---
[21]	CCCCTA	2	0	0	0	2	Yes	Yes	BJT	± 1.75	Yes	Yes	---	---	2.62 MHz	---
[22]	DDCC	1	1	1	0	2	No	No	0.18 µm	± 0.9	Yes	Yes	0.159	> 5	1.64 MHz	---
[26]	FTFNTA	1	1	1	2	0	Yes	No	0.18 µm	± 1.65	Yes	No	---	---	163 kHz	---
[27]	DXCCTA	1	0	1	0	2	No	Yes	0.18 µm	± 1.25	No	Yes	---	---	40 MHz	---
[28]	FDCCII	1	1	1	0	2	Yes	No	0.35 µm	± 1.65	No	Yes	---	---	1 MHz	---
Proposed work	DV-EXCCCII	1	0	0	0	2	Yes	Yes	0.18 µm	± 0.9	No	Yes	2.05	> 6	3.9 MHz	678 µm2

Table 2 Transistor dimensions of DV-EXCCCII

Transistors	W(µm)/L(µm)
M1-M3	12/0.5
M4-M6	16/0.5
M7-M20	12/0.5
M21-M24	10/0.5
M25-M37	20/0.5

Fig. 5(a) represents the frequency response of LPF, HPF, BPF, and BRF. Whereas Fig. 5(b) depicts the magnitude and phase variation of the all-pass filter against frequency. The attenuation at the low frequencies is due to the parasitic elements of DV-EXCCCII. Fig. 6 represents the transient analysis of the circuit. A sinusoidal input of 3.9 MHz and amplitude of 50 µA is applied to APF, which results in 1800 phase-shifted output that confirms the theoretical concept.



(a) Magnitude response of LPF, HPF, BPF, and BRF (b) Magnitude and phase response of APF

Fig. 5 Frequency response of the proposed filter

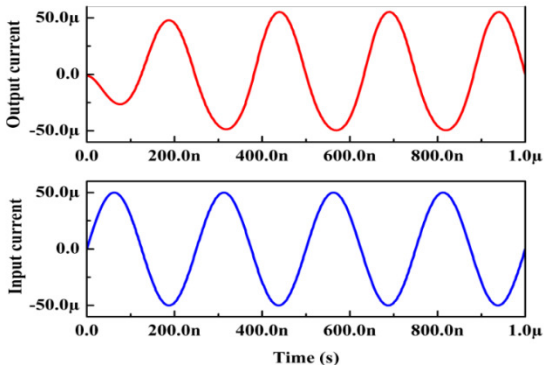
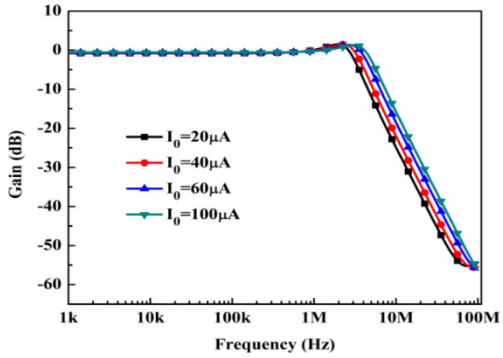
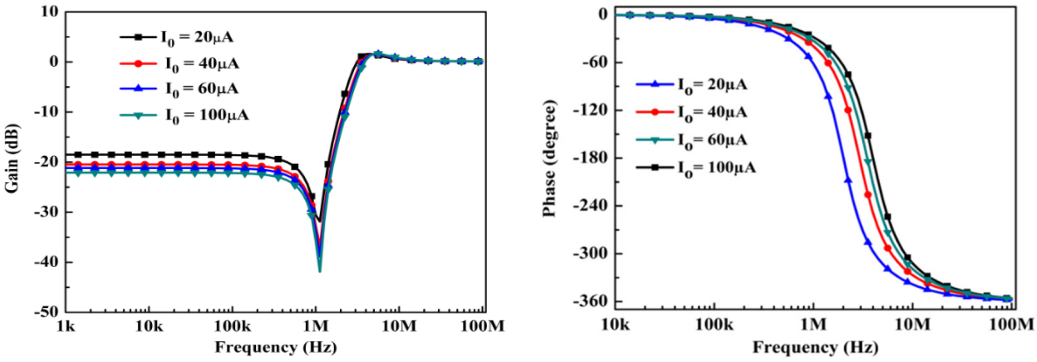


Fig. 6 Time-domain response of the proposed current-mode APF

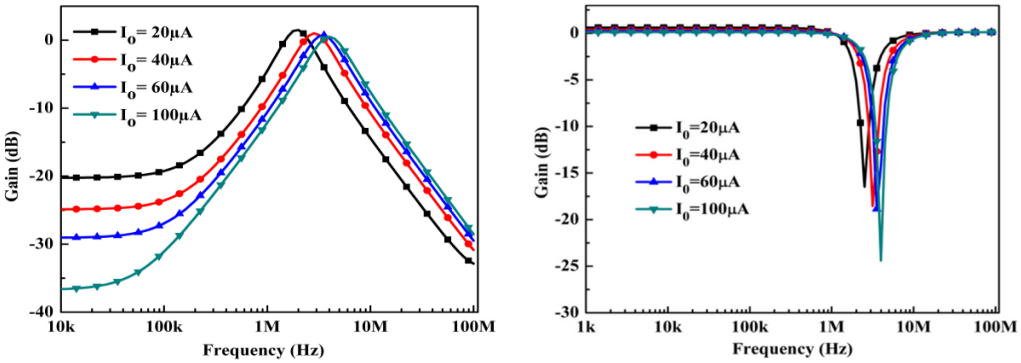


(a) LPF



(b) HPF (c) APF

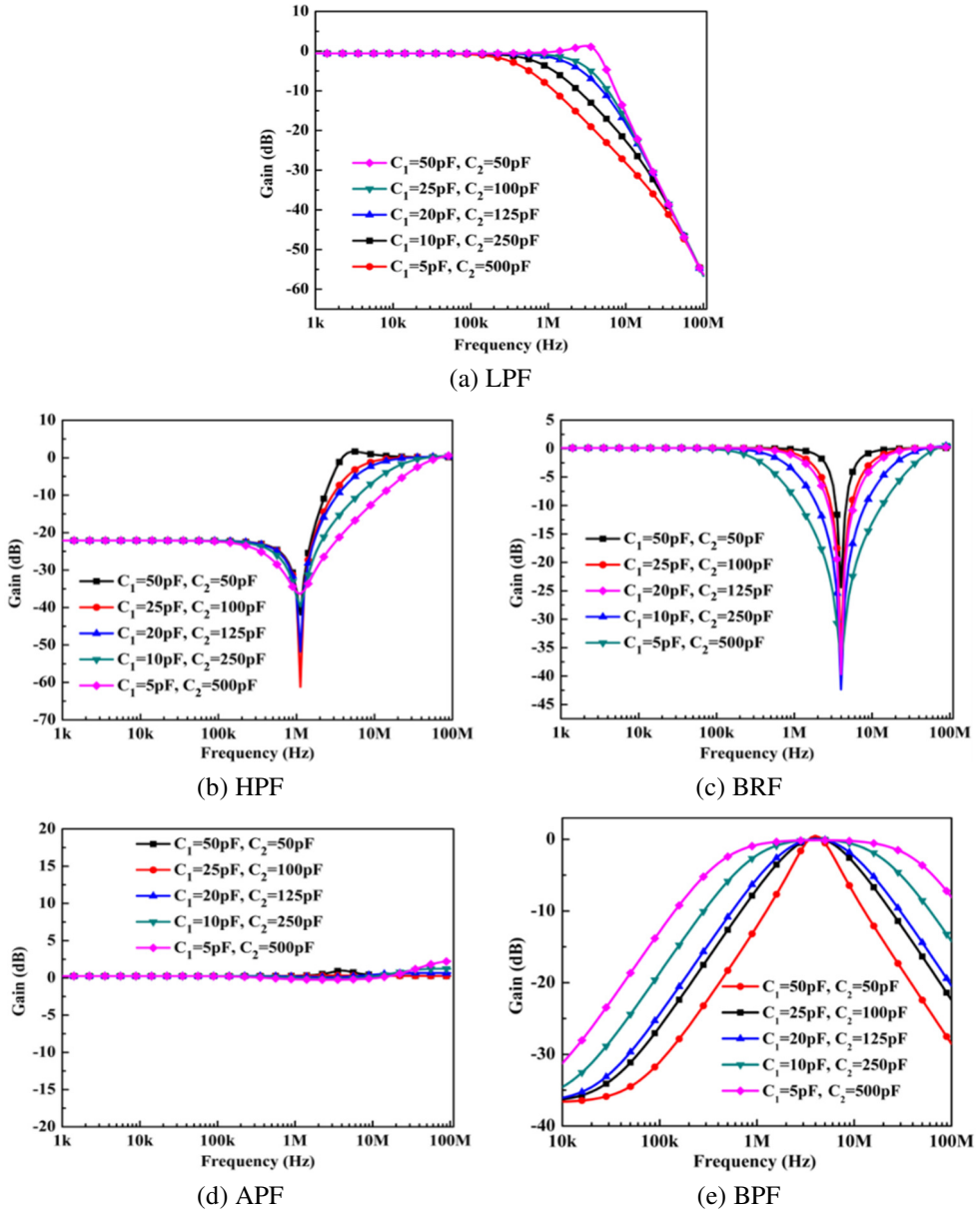
Fig. 7 Electronic tuning characteristics using different I_0



(d) BPF (e) BRF

Fig. 7 Electronic tuning characteristics using different I_0 (continued)

Fig. 7 shows the tunable characteristic of the presented filter by using different bias currents. Fig. 7(c) shows the phase variation of APF at distinct bias currents, whereas Figs. 7(a), (b), (d), and (e) depict the magnitude responses for different I_0 of LPF, HPF, BPF, and BRF, respectively. The quality factor can be tuned by taking various C1 and C2 values. In this way, Q can be tuned independently with ω_0. Fig. 8 shows the frequency response of the proposed filter by choosing various combinations of C1 and C2. The gain response of LPF, HPF, BRF, APF, and BPF is shown in Figs. 8 (a), (b), (c), (d), and (e), respectively.



(a) LPF

(b) HPF (c) BRF

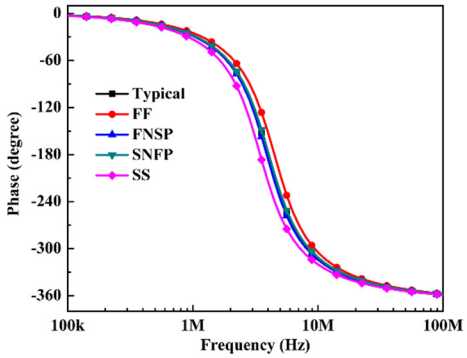
(d) APF (e) BPF

Fig. 8 Magnitude response for different capacitors

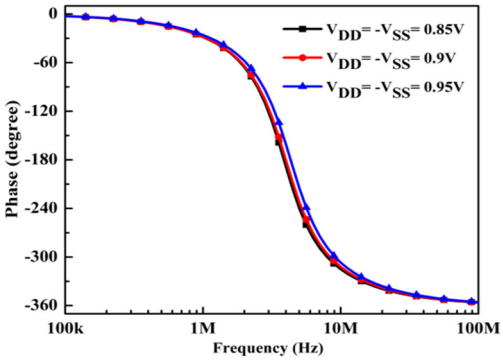
Next, the effect of the process, supply, and temperature variations on the APF phase response is represented. Fig. 9(a) illustrates the phase response of APF at different process corners. The five different corners taken for simulation are Typical, fast-fast (FF), fast n-MOS slow p-MOS (FNSP), slow n-MOS fast p-MOS (SNFP), and slow-slow (SS). The supply voltage variation effect on the proposed filter is shown in Fig. 9(b) using different supply voltages as V_{DD} = -V_{SS} = 0.95 V, 0.9 V, and 0.85 V. The effect of temperature on the filter response can be examined by using various temperature levels. Fig. 9(c) shows the temperature variation effect using temperature values as -50°C, 0°C, 27°C, and 50°C. Table 3 summarizes the pole frequencies of APF due to process, voltage, and temperature variations.

Table 3 Pole frequency of APF for different corners, voltages, and temperatures

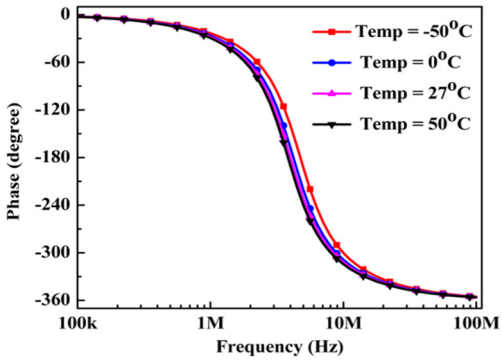
Variation	Different values	Pole frequency (MHz)
Process	Typical	3.98
	FF	4.26
	FNSP	3.90
	SNFP	3.92
	SS	3.74
Voltage	V_{DD} = -V_{SS} = 0.85 V	3.54
	V_{DD} = -V_{SS} = 0.9 V	3.98
	V_{DD} = -V_{SS} = 0.95 V	4.32
Temperature	-50°C	4.43
	0°C	4.22
	27°C	3.98
	50°C	3.87



(a) Process variation



(b) Supply variation



(c) Temperature variation

Fig. 9 Phase response of APF at different variations

The Monte-Carlo analysis is performed with 500 runs for the center frequency of BPF to test the filter performance against process variation. The histogram is shown in Fig. 10 for BPF with a mean value of 3.93 MHz. The mean value slightly deviates from the theoretical value. The noise immunity of the circuit is investigated next. Fig. 11 shows the input and output noise of BPF with a 1 kΩ load resistor. Tables 4 and 5 show the input and output noise of the BPF at different process corners.

Table 4 summarizes the input and output noise at different frequencies for 100 µA input current. In addition, Table 5 represents the input and output noise for different bias currents at 1 Hz frequency. The values show that the noise increases with the bias current and decreases with frequency.

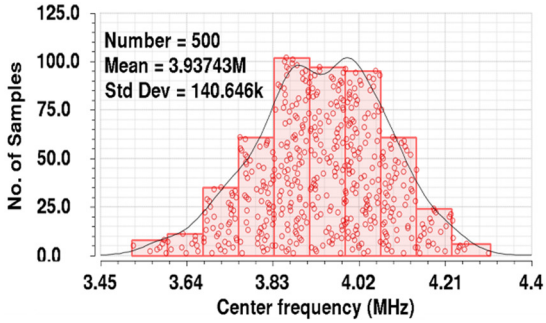
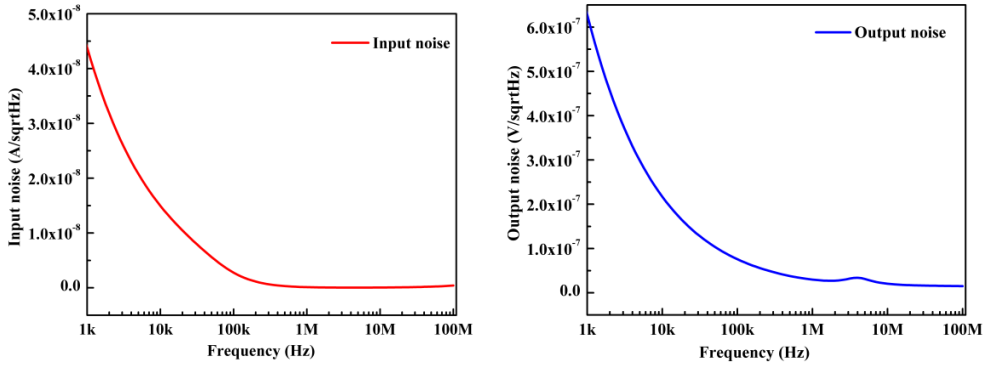


Fig. 10 Monte Carlo simulation result for BPF



(a) Input noise (b) Output noise

Fig. 11 Frequency response of noise of BPF

Table 4 Noise at various corners for different frequencies at 100 µA bias current

Frequency	Input noise (I_N) (A/√Hz) Output noise (O_N) (V/√Hz)	Different process corners				
		Typical	FF	FNSP	SNFP	SS
1 MHz	I_N	3.02×10^{-5}	2.39×10^{-5}	2.37×10^{-5}	3.93×10^{-5}	3.94×10^{-5}
	O_N	4.33×10^{-4}	4.92×10^{-4}	4.19×10^{-4}	4.45×10^{-4}	3.66×10^{-4}
1 Hz	I_N	1.09×10^{-6}	8.63×10^{-7}	8.61×10^{-7}	1.4×10^{-6}	1.41×10^{-6}
	O_N	1.56×10^{-5}	1.78×10^{-5}	1.53×10^{-5}	1.59×10^{-5}	1.32×10^{-5}
1 kHz	I_N	4.38×10^{-8}	3.46×10^{-8}	3.46×10^{-8}	5.63×10^{-8}	5.66×10^{-8}
	O_N	6.27×10^{-7}	7.15×10^{-7}	6.14×10^{-7}	6.38×10^{-7}	5.28×10^{-7}
100 kHz	I_N	2.76×10^{-9}	2.93×10^{-9}	$2.50\times x10^{-9}$	2.99×10^{-9}	2.25×10^{-9}
	O_N	7.58×10^{-8}	8.62×10^{-8}	7.42×10^{-8}	7.70×10^{-8}	6.4×10^{-8}
1 MHz	I_N	1.23×10^{-10}	1.53×10^{-10}	1.18×10^{-10}	1.26×10^{-10}	9.24×10^{-11}
	O_N	2.98×10^{-8}	3.31×10^{-8}	2.93×10^{-8}	3.02×10^{-8}	2.61×10^{-8}
100 MHz	I_N	4.14×10^{-10}	3.97×10^{-10}	4.13×10^{-10}	4.17×10^{-10}	4.36×10^{-10}
	O_N	1.52×10^{-8}	1.65×10^{-8}	1.46×10^{-8}	1.57×10^{-8}	1.37×10^{-8}

Table 5 Noise at various corners for different bias currents at 1 Hz frequency

Bias current	Input noise (I_N) (A/√Hz) Output noise (O_N) (V/√Hz)	Different process corners				
		Typical	FF	FNSP	SNFP	SS
20 µA	I_N	39.54×10^{-9}	36.03×10^{-9}	38.87×10^{-9}	40.24×10^{-9}	44.65×10^{-9}
	O_N	3.8×10^{-6}	4.03×10^{-6}	3.84×10^{-6}	3.79×10^{-6}	3.59×10^{-6}
40 µA	I_N	129.2×10^{-9}	112.0×10^{-9}	126.3×10^{-9}	132.0×10^{-9}	156.2×10^{-9}
	O_N	7.23×10^{-6}	7.77×10^{-6}	7.38×10^{-6}	7.18×10^{-6}	6.74×10^{-6}
60 µA	I_N	320.8×10^{-9}	243.6×10^{-9}	282.7×10^{-9}	342.3×10^{-9}	420.2×10^{-9}
	O_N	11.13×10^{-6}	11.15×10^{-6}	10.41×10^{-6}	11.24×10^{-6}	10.22×10^{-6}
100 µA	I_N	1.09×10^{-6}	8.63×10^{-7}	8.61×10^{-7}	1.4×10^{-6}	1.41×10^{-6}
	O_N	1.56×10^{-5}	1.78×10^{-5}	1.53×10^{-5}	1.59×10^{-5}	1.32×10^{-5}

Fig. 12 shows the total harmonic distortion (THD) variation of the output of BPF. A peak-to-peak sinusoidal input is applied at a 3.9 MHz frequency. The curve of Fig. 12 shows that the THD increases with the applied input current. Fig. 13 shows the layout of DV-EXCCCII, which has an area occupancy of 45.2 m 15 m. The suggested universal filter is also subjected to a post-layout simulation. Fig. 14(a) shows the post-layout gain response of LPF, HPF BPF, and BRF. Fig. 14(b) depicts the post-layout gain and phase response of APF.

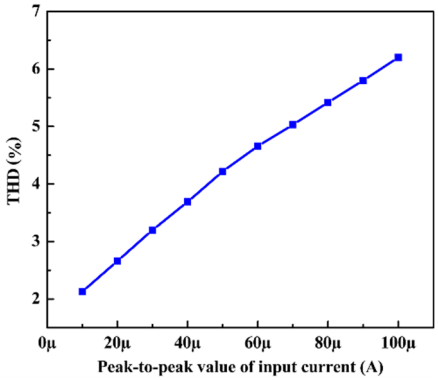


Fig. 12 THD variation of BPF

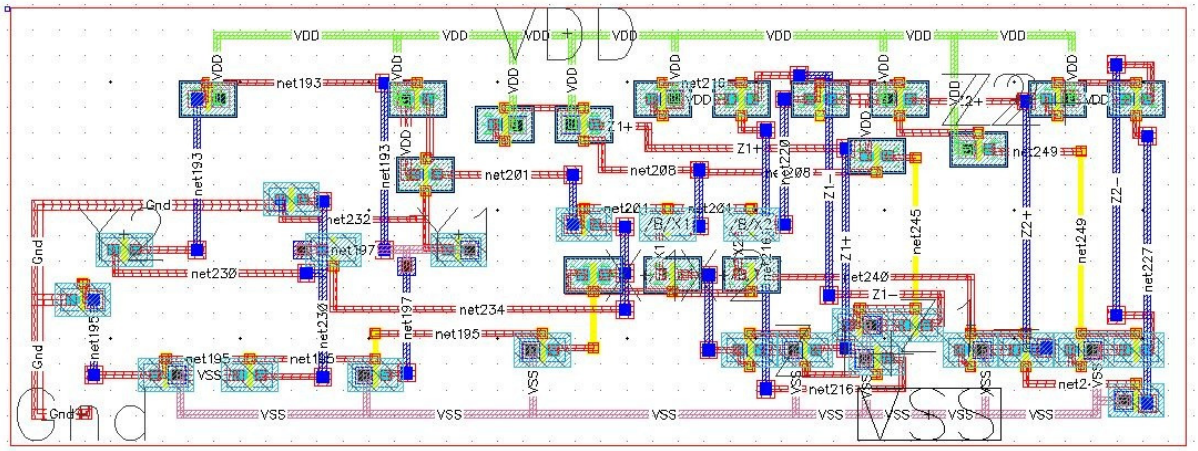
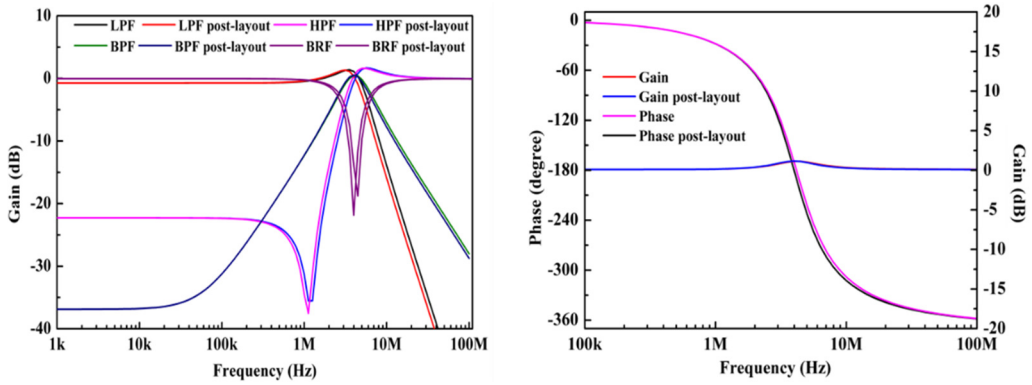


Fig. 13. Layout of DV-EXCCCII



(a) Gain response of LPF, HPF, BPF, and BRF (b) Gain and phase response of APF

Fig. 14. Post-layout simulation of the proposed circuit

6. Practical Consideration

The proposed CMOS-based active element DV-EXCCCII can be practically realized with commercially available CFOA (IC AD844). Fig. 15 represents the implementation of DV-EXCCCII using IC AD844. An ideal AD844 has zero input resistance at the inverting terminal and infinite resistance at the non-inverting and Z terminals. Furthermore, the voltage applied at the non-inverting terminal is reflected at the inverting terminal due to the virtual short effect. The current applied to

the inverting terminal is reflected at terminal Z. To obtain the differential voltage, two AD844s are connected through a resistor R_1 at their inverting terminals. The voltage signals are applied at the non-inverting terminals. The terminal Z of the first AD844 is further connected to the non-inverting terminals of the third and fourth AD844. The following analysis can obtain the voltages at the X1 and X2 terminal in Fig. 15.

$$I_{Y1} = I_{Y2} = 0 \tag{48}$$

$$I_{Z1+} = I_{X1} \tag{49}$$

$$I_{Z2+} = I_{X2} \tag{50}$$

$$I_2 = I_1 = \frac{V_{Y1} - V_{Y2}}{R_1} \tag{51}$$

$$V_{X1} = V_{X2} = I_2 R_2 = \frac{R_2}{R_1}(V_{Y1} - V_{Y2}) \tag{52}$$

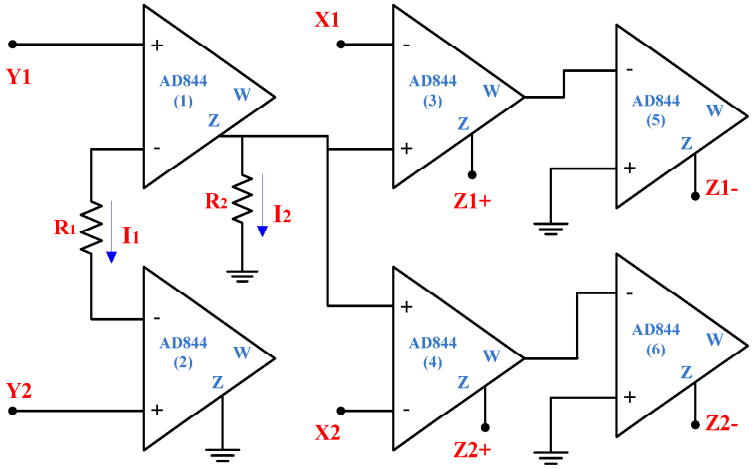


Fig. 15 DV-EXCCCII implementation using IC AD844

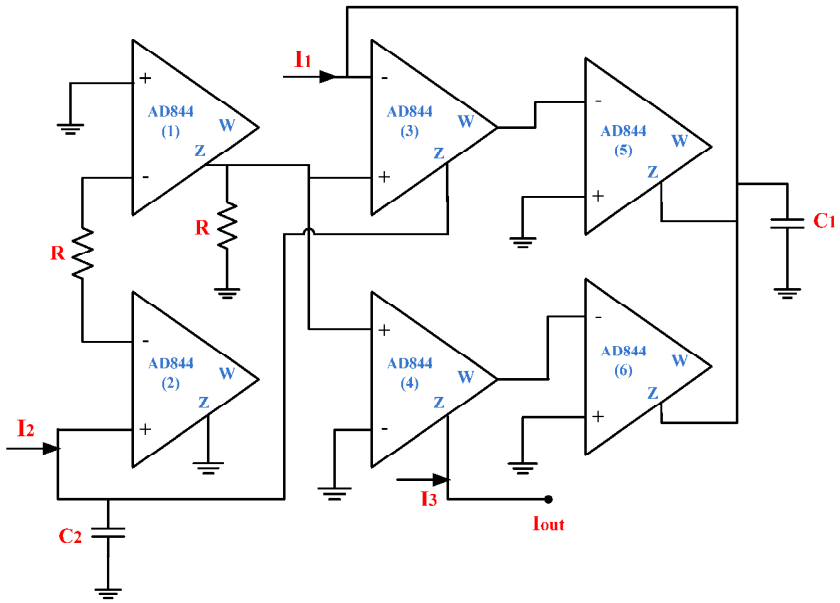


Fig. 16 Implementation of the proposed circuit using IC AD844

Eq. (52) shows that the differential voltage at terminals X1 and X2 of Fig. 15 can be obtained if R_1=R_2 is set. Fig. 16 shows the implementation of the proposed circuit using IC 844. The proposed universal filter shown in Fig. 3 is practically

realized with the IC AD844 model in the LTSPICE tool. Fig. 17 shows the time-domain response of the APF with a sinusoidal input of an amplitude of 100 µA at 3.9 MHz. The output obtained is 180° phase-shifted with the applied input signal. The result confirms the theoretical concept of the filter. Fig. 18 shows the THD variation of APF with a peak-to-peak sinusoidal input of 3.9 MHz. This curve indicates that the THD increases with the applied input current.

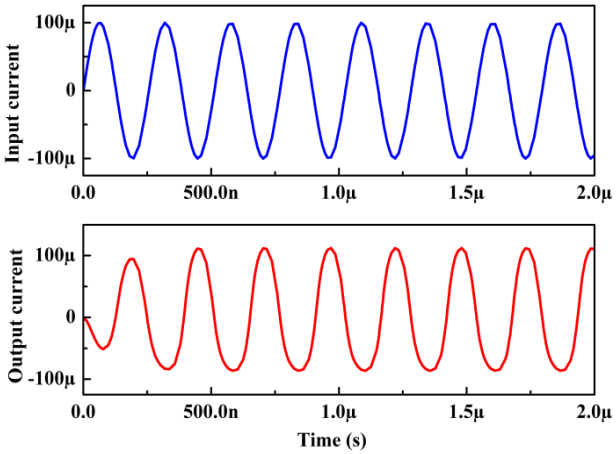


Fig. 17 Transient response of APF using IC AD844

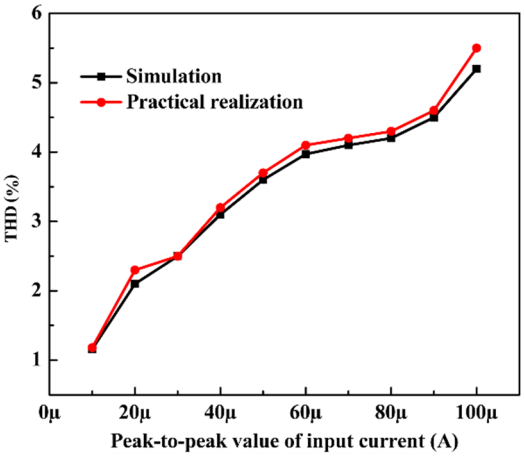


Fig. 18 THD variation of APF

7. Conclusion

This study presents a resistor-less universal filter using one DV-EXCCCII and two capacitors. This circuit can implement all fundamental filters of a biquadratic filter with the same circuit configuration without passive component matching constraints. This circuit is electronically tunable, and also it is cascadable because of its high output impedance. The non-ideal analysis and Monte Carlo simulation are performed to indicate the satisfactory response of the proposed circuit under the influence of non-idealities and mismatches. The presented filter circuit is verified using Cadence Spectre, and the simulation results of the proposed filter are found to be in good agreement with the proposed theory.

Conflicts of Interest

The authors declare no conflict of interest.

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