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# Field Programmable Gate Array (FPGA) Model of Intelligent Traffic Light System with Saving Power

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## Abstract

In this paper, a FPGA model of intelligent traffic light system with power saving was built. The intelligent traffic light system consists of sensors placed on the side's ends of the intersection to sense the presence or absence of vehicles. This system reduces the waiting time when the traffic light is red, through the transition from traffic light state to the other state, when the first state spends a lot of time, because there are no more vehicles. The proposed system is built using VHDL, simulated using Xilinx ISE 9.2i package, and implemented using Spartan-3A XC3S700A FPGA kit. Implementation and Simulation behavioral model results show that the proposed intelligent traffic light system model satisfies the specified operational requirements.

*Keywords:* Intelligent Traffic light system, Intelligent Traffic light controllers, Traffic light algorithm, FPGA, Xilinx ISE 9.2i.

### 1. Introduction

Travel became very difficult between the places of the city because of traffic jams. Traffic jams are a major problem in many modern cities around the world. When populations increase, the number of cars is increasing. Therefore, traffic congestion is growing. Traffic jams lead to a loss of time for people, the loss of opportunity, and nervous tension.

Most traffic light controllers are fixed-cycle controllers, in which all alternative traffic light settings get a particular time-interval for being green. [1]

In the fixed time traffic light control system, cannot get the optimal solution for the traffic congestion. This leads to using other systems. One of these systems is an intelligent traffic light system. [2]

Most of the traffic light systems operate depending on the specific time for each specific light. An intelligent traffic light system senses the presence or absence of vehicles and reacts accordingly. The idea behind the intelligent traffic systems is to reduce unnecessary waiting time for drivers when the light is red. The intelligent traffic system detecting the presence or absence of vehicles, determines the time required for each side. There are several ways to detect the presence of vehicles on the roads. [3-4]

A different approach based on applying intelligent traffic systems in order to manage traffic flow in a more effective and efficient manner is needed. [5-6]

Sensor is a crucial element in an intelligent traffic control. The most common sensor is inductive loop. It is very common in vehicle actuated system to detect vehicle presence. It is also very common in an urban traffic control system to count the number or to measure headway of approaching vehicles. Another type of sensor is video detection system. This system is very flexible and able to carry out traffic count and measure queue length accurately. [5-7]

Recently, FPGAs have been seen to support real-time network traffic measurements [8]. The FPGA is a suitable platform for accelerating scientific computations. FPGAs are a good alternative to application specific integrated circuits (ASICs) for high speed embedded MPC applications since they offer much reduced lowvolume cost, greater flexibility, and a shorter design cycle, reducing the risk while still maintaining deterministic execution time and high power efficiency [9].

The aim of this paper is to design a new approach of intelligent traffic light system with saving power based on FPGA. This system operates according to the number of vehicles on each side of the intersection instead of using a fixed time for each traffic light (green, yellow, and red). So this system will work like a traffic cop when governing the passage of vehicles. Therefore, it will reduce the waiting time.

# 2. The Proposed Intelligent Traffic Light System

The proposed intelligent traffic light system consists of sensors placed on each side ends of the intersection. These sensors are sensitive to the presence or absence of vehicles. The sensors are responsible for the account of vehicles entering the road, as well as outside of it, hence the number of vehicles on each side calculated by the FPGA IC according to equation (1). It is possible to use any type of sensors.

$$C_n = Cin_n - Cout_n \qquad \dots (1)$$

whre

 $C_n$  is the number of vehicles on side *n*. Cin<sub>n</sub> is the number of vehicles entering th side *n*.

| <i>Cout</i> <sub>n</sub> | is | the | number | of | vehicles | coming | out | of |
|--------------------------|----|-----|--------|----|----------|--------|-----|----|
| side n.                  |    |     |        |    |          | -      |     |    |

So when  $C_n$  is equal to zero; it means that side *n* is empty.

For the sub-street, the sensors placed at the end with the main street (each side of intersection represents Main Street). These sensors are connected with the main sensors of the Main Street. Thus, any vehicle moving out of the substreet to the Main Street will be calculated as if it entered the main street through the main sensor itself. In other words, the counter of this side will be increment. Furthermore, in the case of vehicles coming out of the main street to the sub-street; the counter will be decrement.

Figure (1) illustrates the mechanism of the development of the sensors on both ends of each side of the intersection.

The proposed system works with nine states as shown in Table (1). As observed in state 0 all Lights are switched off, which represents the power saving state. Power saving occurs when the lights of traffic are switched off so no power is consumed thus it depends on the absence of vehicles in the intersection. The other states represent the normal operation of the traffic light system. In this system, the transition from one state to another is not sequential. If the sensor detects the absence of vehicles on the sides of the intersection, the lights will be switched off (state 0).

| State | State Description | Traffic 1 | Traffic 2 | Traffic 3 | Traffic 4 |
|-------|-------------------|-----------|-----------|-----------|-----------|
| 0     | Power Save        | off       | off       | off       | off       |
| 1     | Traffic 1 green   | Green     | Red       | Red       | Red       |
| 2     | Traffic 1 yellow  | Yellow    | Red       | Red       | Red       |
| 3     | Traffic 2 green   | Red       | Green     | Red       | Red       |
| 4     | Traffic 2 yellow  | Red       | Yellow    | Red       | Red       |
| 5     | Traffic 3 green   | Red       | Red       | Green     | Red       |
| 6     | Traffic 3 yellow  | Red       | Red       | Yellow    | Red       |
| 7     | Traffic 4 green   | Red       | Red       | Red       | Green     |
| 8     | Traffic 4 yellow  | Red       | Red       | Red       | Yellow    |

| Table 1,                                    |  |
|---|--|
| States of Intelligent Traffic Light System. |  |

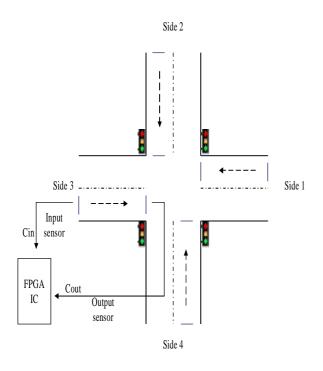


Fig. 1. Mechanism of Sensors on Both Ends of Each Side of the Intersection.

This system is also a transition from state to state depending on the presence of vehicles on the road. In the absence of vehicles on a specific side, this side will be neglected (the green light does not work). In the event that the green light was on and all vehicles passed, the system will go to the other state without going through the yellow light state. If one side of the intersection has many vehicles and too 60 seconds passied (including yellow light state), the system will go to the other state, to prevent a long wait on the other sides of the intersection. Transition to another state does not occur if one side is filled with vehicles and the other sides. Are empty. All these conditions lead to reduce waiting time at the intersection when the red light was on.

In case of vehicle failure on one side of the intersection, this side will take its normal passing time of 60 seconds before turning to the next, because the counter on this side did not specify that this side was empty. The operations of the proposed model are demonstrated in the flowchart shown in Figure (2).

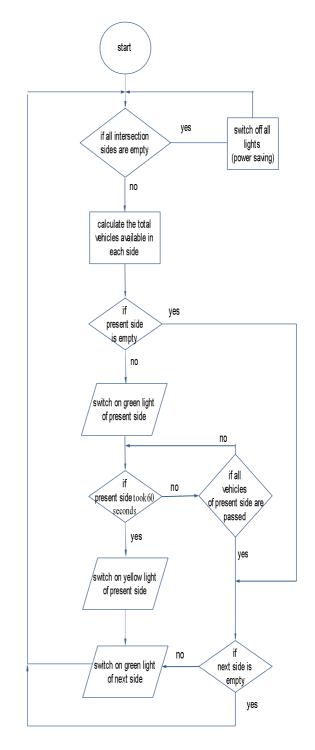


Fig. 2. The Flowchart of the Proposed Traffic Light.

#### 3. FPGA Model of Intelligent Traffic Light System

The FPGA model of intelligent traffic light system is built using VHDL (Very high speed Hardware Description Language), and implemented and simulated using Xilinx ISE 9.2i package. This model consists of two parts, entity declaration and process. The entity declaration part, shown in Figure (3), is used to declare the signals of the intelligent traffic light system. The process part will be responsible for the processing traffic light system signals under the conditions described previously, and control the illuminations of traffic light according to system state.

Figure (4) shows the intelligent traffic light signals; the input signals (Cin1, Cin2, Cin3, and Cin4) represent the car input that is received by the signal the sensor to indicate that the vehicle entered that side of intersection. Car output (Cout1, Cout2, Cout3, and Cout4); its input signals coming from a sensor as an indicator that the vehicle coming out of the intersection. The lights of the traffic light system are controlled by the output signals (R1, Y1, G1, R2, Y2, G2, R3, Y3, G3, R4, Y4, and G4).

The simulation behavioral model test results of the intelligent traffic light system are shown in Figures (5 to 8). As illustrated in Figure (5) when a vehicle entered a specific side and the other sides of the intersection were empty, the green light of this side will be illuminated directly to facilitate the passage of the vehicle without waiting.

If one side completed the passage of all the vehicles that were on it, the system will go to the other state without going through a yellow light state, as cleared in Figure (6).

Figure (7) indicates that the system does not pass to any other state if one side of the intersection is of vehicles and the other sides are empty. As shown in Figure (8), if one side of the intersection ha exceeded the time desired, it will transmit to the yellow light state and then to the other state depending on the presence of vehicles on other sides.

As noted in the Figures (5 to 8) the saving power state is clear, occurs when all sides of the intersection are empty.

Figure (9) illustrates the implementation of the proposed model where a prototype of traffic lights system was used. A push-bottom sensor is placed on the sides ends to detect the absence and the presence of vehicles; therefore sends it the signals to the Spartan-3A XC3S700A FPGA kit. The kit will count the number of vehicles depending on equation (1) and activate each side according to suitable state.

The number of vehicles can pass in a specific side through a one period when the other sides are

empty as shown in Figure (10). As noted, the number of vehicles in the fixed-time system remains constant, while the number of vehicles triples when using the proposed system. Figure (11) shows the number of vehicles that can pass in a specific side compared to the available vehicles in other sides. As observed, it is possible to pass 240 vehicles on one side, if the other sides are empty in case of using the proposed model, while it does not exceed 60 vehicles when using the Fixed-time system.

There are many avails of using the proposed model over the other traffic lights systems; it is easy maintenance because it uses one IC, unlike some systems that use more components [1]. The proposed system depends on a simple algorithms and equations while other system based on complicate algorithms like JADE [3] and Fuzzy Logic [4]. Moreover, most of other systems use computer to control them traffic lights and this make it more liable to be exposed to hacking and system errors [2,6]. Also, it uses any type of sensors, unlike some other systems that require specific types of sensors.

| ontitu ITTI ia                      |
|-------------------------------------|
| entity ITL is                       |
| <pre>port(clock:in std_logic;</pre> |
| Cin1:in std_logic;                  |
| Coutl:in std_logic;                 |
| Cin2:in std_logic;                  |
| Cout2:in std_logic;                 |
| Cin3:in std_logic;                  |
| Cout3:in std_logic;                 |
| Cin4:in std logic;                  |
| Cout4:in std_logic;                 |
| R1:out std logic;                   |
| Y1:out std logic;                   |
| G1:out std_logic;                   |
| R2:out std_logic;                   |
| Y2:out std logic;                   |
| G2:out std_logic;                   |
|                                     |
| R3:out std_logic;                   |
| Y3:out std_logic;                   |
| G3:out std_logic;                   |
| R4:out std_logic;                   |
| Y4:out std_logic;                   |
| G4:out std_logic                    |
| ;)                                  |
| end ITL;                            |
|                                     |

Fig. 3. The Entity Source Code Declaration.

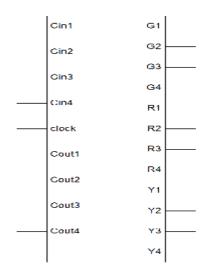


Fig. 4. Intelligent Traffic Light Signals.

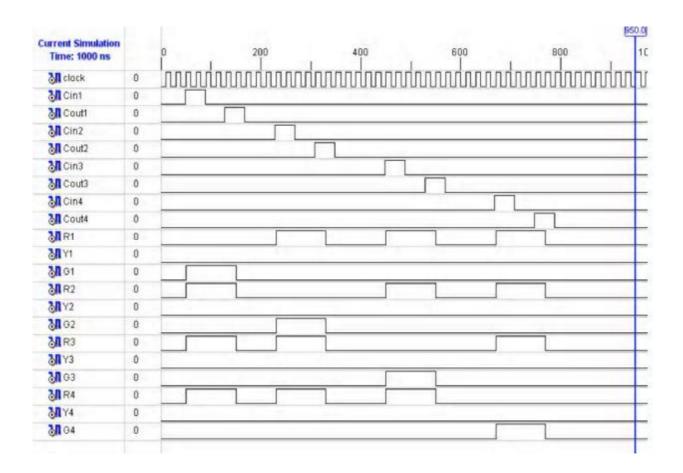


Fig. 5. Simulation Behavioral Model when One Side has Vehicles and others are Empty.

| Current Simulation<br>Time: 1000 ns |   | 0 200 400 600 800                           |
|-------------------------------------|---|---|
| Clock                               | 0 | ກກ່ານການການການການການການການການການການການການກາ |
| Cin1                                | 0 |   |
| Cout1                               | 0 |   |
| Cin2                                | 0 |   |
| Cout2                               | 0 |   |
| Cin3                                | 0 |   |
| Cout3                               | 0 |   |
| M Cin4                              | 0 |   |
| Cout4                               | 0 |   |
|                                     | 0 |   |
| 31 Y1                               | Ú |   |
| 31 G1                               | 0 |   |
| 3 R2                                | 0 |   |
| 31Y2                                | 0 |   |
| M G2                                | 0 |   |
| MR3                                 | 0 |   |
| 31 Y3                               | 0 |   |
| 31 G3                               | 0 |   |
| MR4                                 | 0 |   |
| 31 Y4                               | 0 |   |
| 30 G4                               | 0 |   |

Fig.6. Simulation Behavioral Model when One Side had Completed Passage of all Vehicles and the others have Vehicles.

| Current Simulation<br>Time: 1000 ns |   | 0 200 400 600 800 1 |
|-------------------------------------|---|---------------------|
| SI clock                            | 0 |                     |
| Cin1                                | 0 |                     |
| Coutt                               | 0 |                     |
| Cin2                                | 1 |                     |
| Cout2                               | 0 |                     |
| Cin3                                | 0 |                     |
| SA Cout3                            | 0 |                     |
| Cin4                                | 0 |                     |
| Cout4                               | 0 |                     |
| UR1                                 | 1 |                     |
| 30 Y1                               | 0 |                     |
| 30 G1                               | 0 |                     |
| MR2                                 | 0 |                     |
| SAY2                                | 0 |                     |
| 30 02                               | 1 |                     |
| MR3                                 | 1 |                     |
| 31 Y3                               | 0 |                     |
| 31 G3                               | 0 |                     |
| MR4                                 | 1 |                     |
| 31 Y4                               | 0 |                     |
| 30 64                               | 0 |                     |

Fig. 7. Simulation Behavioral Model when one Side is full and others is Empty.

| urrent Simulation<br>Time: 1000 ns |   | 0 200 400 600 800  | 1   |
|------------------------------------|---|--|-----|
| an clock                           | 0 | ່ກການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການກ່ານການການການການການການການການການການການການກາ | ппг |
| Cin1                               | 0 |  |     |
| Coutt                              | 1 |  | _   |
| Cin2                               | 0 |  |     |
| Cout2                              | 0 |  |     |
| Cin3                               | 0 |  |     |
| Cout3                              | 0 |  |     |
| Cin4                               | 0 |  | _   |
| Cout4                              | 0 |  |     |
| MR1                                | 0 |  |     |
| 31Y1                               | 0 |  |     |
| 30 G1                              | 1 |  |     |
| MR2                                | 1 |  |     |
| MY2                                | 0 |  |     |
| 30 02                              | 0 |  |     |
| MR3                                | 1 |  |     |
| MY3                                | 0 |  |     |
| 30 03                              | 0 |  | _   |
| MR4                                | 1 |  |     |
| SR Y4                              | 0 |  |     |
| 30 64                              | 0 |  | _   |

#### Fig. 8. Simulation Behavioral Model When One Side Is Full And Exceeds The Time Desired.



Fig.9. The Proposed Model Implementation Using the Spartan-3A XC3S700A FPGA kit.

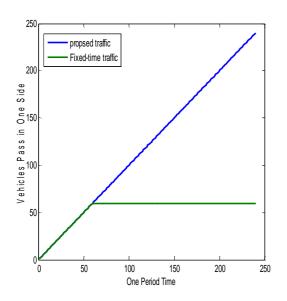


Fig. 10. The Number of Vehicles Passed in One Side through a One Period when the other Sides are Empty.

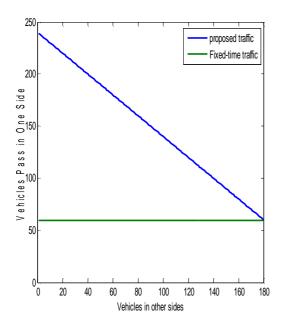


Fig. 11. The Number of Vehicles Passed in One Side Compared to the Available Vehicles in other Sides.

#### 4. Conclusions

The traditional traffic light system wasted a lot of time because it has a fixed interval time, and does not depend on the number of vehicles in the sides of intersection. To reduce the wasted time another approach must be used. The best approach and best solution to minimize the lost time is the intelligent traffic light system.

In this paper, the FPGA model of a proposed design intelligent traffic light system with saving power has been presented. The intelligent traffic light system is illuminating traffic lights according to the presence or absence of vehicles on the sides of the intersection. This system is disposal any lost time through the transition from one traffic light state to another when the state is not useful and useless time. So the waiting time of red light will reduce. Furthermore, the system will turn off all traffic lights when it senses the absence of vehicles at all sides of intersection to save the power. Results showed that the proposed system is able to pass three times the number of vehicles of fixed-time system in a one side when the other sides are empty.

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# نموذج (FPGO) لنظام الاشارات المرورية الذكي الحافظ للطاقة الكهربائية

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#### الخلاصة

تم بناء نموذج FPGA لنظام الإشارات المروية الذكي الحافظ للطاقة الكهربائية. يتكون نظام الإشارات المرورية الذكي من متحسسات توضع على أطراف جوانب التقاطع لتحسس وجود أو غياب المركبات. يقوم هذا النظام على تقليل وقت الانتظار عندما يكون ضوء الإشارة المرورية حمراء، وذلك من خلال الانتقال من حالة ضوئية مرورية إلى حالة أخرى عندما تكون الحالة الأولى تهدر الوقت، وذلك لعدم وجود المركبات فيها. تم بناء هذا النظام باستخدام لغة الـ VHDL وتم محاكاته باستخدام Xilinx ISE 9.2i package ، وتنفيذه باستخدام لفا التشعيلية المركبات فيها. تم بناء هذا النظام باستخدام نتائج محاكاة هذا النموذج بان نظام الإشارات المروية الذكي المقترح قد حقق المتطلبات التشغيلية المحددة.