Al-Khwarizmi Engineering Journal, Vol. 4, No. 3, PP 1-7 (2008)

Al-Khwarizmi Engineering Journal

Design and Simulation of GaussianFSK Transmitter in UHF Band Using Direct Modulation of ΣΔ Modulator Fractional-N Synthesizer

Ali Mohammed Noori Hasan

Departement of Information and Communication/ Al-Khawarizmi College of Engineering /University of Baghdad

(Received 4 March 2008; accepted 21 July 2008)

Abstract

This research involves design and simulation of GaussianFSK transmitter in UHF band using direct modulation of ΣΔ fractional-N synthesizer with the following specifications:

Frequency range (869.9– 900.4) MHz, data rate 150kbps, channel spacing (500 kHz), Switching time 1 µs, & phase noise @10 kHz = -85dBc.

New circuit techniques have been sought to allow increased integration of radio transmitters and receivers, along with new radio architectures that take advantage of such techniques. Characteristics such as low power operation, small size, and low cost have become the dominant design criteria by which these systems are judged.

A direct modulation by ΣΔ fractional-N synthesizer is proposed in this research, because this approach provides the required characteristics such as low power. The ΣΔ modulator placed on digital phase-locked loop to control the fractional value of the frequency division ratio thereby eliminating spurious and allowing good phase noise performance. The modulation type of Gaussian FSK is used to obtain high spectral efficiency of modulated waveform.

The applications of this transmitter in low cost wireless data transfer, security systems, RF remote controls and wireless metering.

Keywords: Mash modulator, Gaussian, fractional, sigma deta and FSK.

1. Introduction:

The use of wireless products has been rapidly increasing the last few years, and there has been world wide development of new systems to meet the needs of this growing market. Characteristics such as low power operation, small size, and low cost have become the dominant design criteria by which these systems are judged. As a result, new circuit techniques have been sought to allow increased integration of radio transmitters and receivers, along with new radio architectures that take advantage of such techniques. Radio transmitters revolve around a common goal—a low frequency modulation signal must be translated to a desired RF band. Since the advent of the superheterodyne design by Armstrong (which dates back to 1918 [1]), the majority of high performance, narrowband transmitters have accomplished this frequency translation using mixers and an intermediate frequency (IF) region of operation to perform highly-selective filtering. While such an approach offers excellent radio performance (low spurious noise for transmitters), it carries with it a high cost of implementation in light of efforts to integrate radio architectures. Specifically, this approach is impeded by the inability to integrate the high-Q, low-noise, low-distortion bandpass filters required at IF frequencies (often on the order of 70 to 100 MHz for 900 MHz systems). For the above reasons, research into non-heterodyne architectures has taken place over the last few years in response to the growing demand for portable communication devices. Indeed, the use of direct carrier modulation has now become widespread in a transmitter [1], which allows the channel shaping filters to be implemented at baseband and thus be integrated.

2. Modulator Architectures:

Of the new designs, the one that appears most promising in terms of power consumption involves the direct modulation of a VCO. Figure (1) displays the basic operations that are used to perform frequency translation in the above designs. The prevalent method, shown in part (a), is to use a mixer to multiply the modulation signal by a periodic waveform produced by a voltage controlled oscillator (VCO) whose frequency is precisely set through the action of a frequency synthesizer. In the case of direct conversion, the modulation waveform is an analog signal composed of I and Q channels which are directly translated from baseband to the desired RF frequency and then added together. The superheterodyne approach uses at least two stages of mixers to accomplish the frequency translation so that an intermediate filtering stage can be employed. As discussed above, the direct conversion method is preferred to achieve high integration. However, it should be noted that this method requires two mixers and D/A converters to accommodate the I and Q channels.

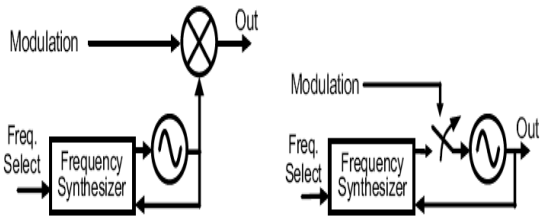

Fig. 1. Two Current Approaches of Modulation Upconversion: (a) Mixer Based, (b) Direct Modulation of VCO.

The removal of all mixers can be accomplished by using the VCO to perform the required frequency translation. As illustrated in part (b) of the figure, the translation is accomplished by injecting the baseband, *analog* modulation signal into the input of the VCO after the frequency synthesizer has guided the VCO output to the desired carrier frequency. Phase and/or frequency modulation of a frequency synthesizer is accomplished by varying its divide value according to input data. A simple method of performing this task is shown in Figure 2. Binary input data selects the divide ratio to be either *N* or *N* +1 depending on whether the input is 0 or 1, and *N* is chosen to achieve the desired carrier frequency. The output frequency settles to *Fout= NFref*, so that binary frequency shift keying (FSK) modulation is produced as *N* is varied. In the figure, the resulting output spectrum is illustrated under the assumption that *Fref* = 20 MHz and that *N* = 90. The carrier frequency is seen to be 1.81 GHz, and the modulation frequency deviation equals *Fref*. Unfortunately, the FSK modulation method depicted in Figure (2) is not practical for most applications due to its inefficient use of spectrum. The spectral efficiency is greatly improved if a smooth transition is made during frequency transitions and the modulation deviation is optimized.

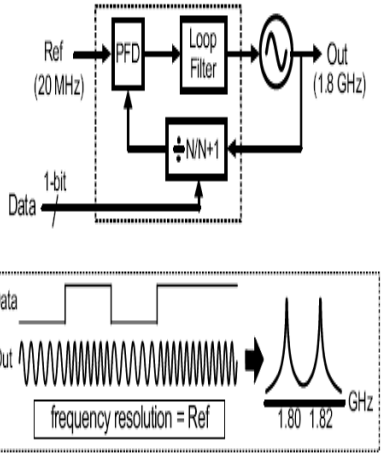

Fig. 2. Direct Modulation of a Frequency Synthesizer.

Figure 3 illustrates a fractional-*N* modulator that achieves high spectral efficiency by using a digital transmit filter to obtain smooth transitions in the modulation data, and a digital Σ-Δ modulator to dither the divide value according to the resulting modulation sequence [2].

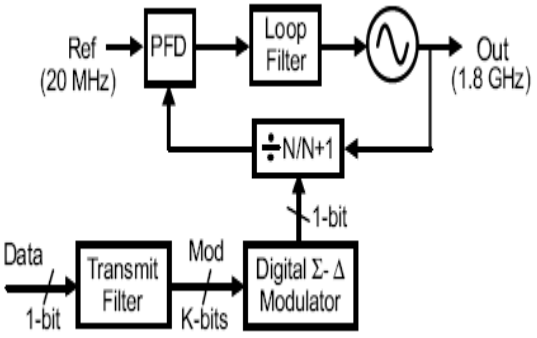

Fig. 3. A Spectrally Efficient, Fractional-*N* Modulator.

Gaussian Frequency Shift Keying, or GFSK, represents a filtered form of frequency shift keying. The data to be modulated to RF is prefiltered digitally using a finite impulse response filter (FIR). The filtered data is then used to modulate the sigma-delta fractional-N to generate spectrally-efficient FSK.

FSK consists of a series of sharp transitions in frequency as the data is switched from one level to another. The sharp switching generates higher frequency components at the output, resulting in a wider output spectrum. With GaussianFSK, the sharp transitions are replaced with up to 128 smaller steps. The result is a gradual change in frequency. As a result, the higher frequency components are reduced and the spectrum occupied is reduced significantly. GFSK does require some additional design work as the data is only sampled once per bit, and so the choice of crystal is important to ensure the correct sampling clock is generated.

3. Sigma Delta Modulation:

This method will be used to implement fractional N synthesizer in this system to eliminate the fractional spurs. The accumulator used to control the modulus of the prescaler can be viewed as the digital counter part of a first-order analog ΣΔ-modulator. The carry of Accumulator changes the prescalar from N to N+1 for one cycle Figure (4) shows the accumulator, i.e. an adder with a one clock cycle delay in the feedback path, with the corresponding signals. The frequency control word is fed into the *A* input, and added to the *B* input to produce a sum output Σ. When the adder overflows, the carry out bit *c* is set[3].

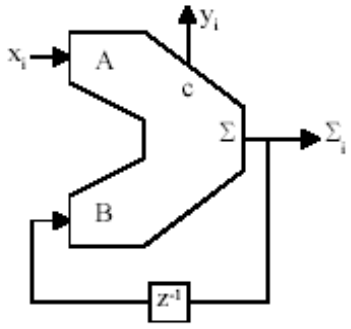

Fig.4. The Digital Accumulator with the Corresponding Input and Output Signals.

Let us denote the frequency control signal fed to input *A* by x_i, and carry output *c* of the accumulator by y_i. When an overflow occurs, the contents of the accumulator are "flipped over", which can be viewed as subtracting the full scale of the accumulator from its contents.

The output of the accumulator at an arbitrary time is the sum of its input at that time and its contents one clock period earlier. If an overflow occurs, the full scale of the accumulator is subtracted. The output can thus be expressed as

$$\Sigma_i = x_i + \Sigma_{i-1} - y_i \quad \ldots(3.1)$$

$$y_i = x_i + \Sigma_{i-1} - \Sigma_i \quad \ldots(3.2)$$

$$y_i = x_i - (\Sigma_i - \Sigma_{i-1}) \quad \ldots(3.3)$$

The z-transform of equation (3-3) is

$$Y(z) = X(z) - \Sigma(z)\,(1 - z^{-1}) \quad \ldots(3.4)$$

Let us now look at the signal flow diagram of a first-order analog ΣΔ-modulator shown in Figure (5). The input is again denoted by *x*, and the output by *y*. The operation performed in the dashed box is the quantization, and *e* denotes the quantization error.

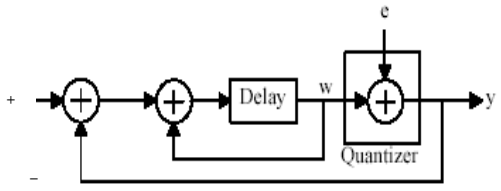

Fig. 5. The Signal Flow Diagram of a First-Order Analog ΣΔ-Modulator.

The above modulator is described by the following equations:

$$w_i = w_{i-1} + x_{i-1} - y_{i-1} \quad \ldots(3.5)$$

$$y_i = w_i + e_i \quad \ldots(3.6)$$

Combining these two, we get

$$y_i - e_i = y_{i-1} - e_{i-1} + x_{i-1} - y_{i-1} \quad \ldots(3.7)$$

$$y_i = x_{i-1} + e_i - e_{i-1} \quad \ldots(3.8)$$

The z-transformation of Equation (3.8) is

$$Y(z) = z^{-1} X(z) + E(z)\,(1 - z^{-1}) \quad \ldots(3.9)$$

Comparing Equation (3.9) with Equation (3.4) shows great similarity. Ignoring the latency of one clock period in the signal path of the analog ΣΔ-modulator, and treating the contents of the digital accumulator as the negative of the quantization error, the equations are identical. The signal in the ΣΔ-output of the accumulator, however, is no longer at DC, although it is periodical. Now, this signal can be fed into the input of another accumulator, whose output will be much less periodic than the output of the first accumulator. The first accumulator carry changes the division ratio of the Divider from N to N+1 for one cycle. The output is digitally integrated by the second accumulator and its carry output changes the division ratio to N+1 and then N-1 on the next clock cycle. Combining the *c* outputs of the two accumulators in a suitable way (see figure 6), the quantization noise of the first accumulator can be canceled [4].

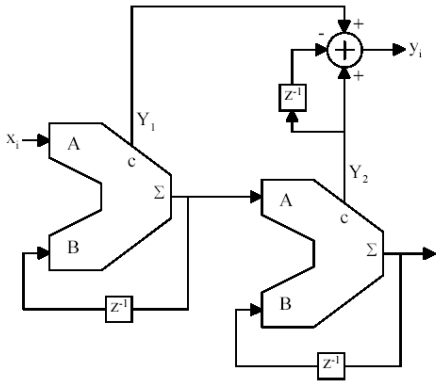

Fig. 6. The Block Diagram of a Second-Order MASH Modulator.

As shown in Equations (3.1) to (3.4), the output of the first accumulator is

$Y_1(z) = X(z) – \Sigma_1(z) (1 – z^{-1})$ …(3.10)

Feeding the Σ -output of the first accumulator into the input of the second one, the output of the second accumulator is

$Y_2(z) = \Sigma_1(z) – \Sigma_2(z) (1 – z^{-1})$ …(3.11)

Combining the outputs of the accumulators as shown in Figure 6, we get the following as the output of the entire modulator:

$Y(z) = Y_1(z) + Y_2(z) – Y_2(z) z^{-1}$ …(3.12)

$Y(z) = Y_1(z) + Y_2(z) (1 – z^{-1})$ …(3.13)

$Y(z) = X(z) - \Sigma_1(z) (1 – z^{-1}) + \Sigma_1(z) (1 – z^{-1}) - \Sigma_2(z) (1 – z^{-1})$ …(3.14)

$Y(z) = X(z) - \Sigma_2(z) (1 – z^{-1})^2$ …(3.15)

As Equation (3.15) shows, the quantization noise of the first accumulator cancels out. This greatly improves the spurious performance of the modulator, since the first accumulator is the one with the more periodical output. Also, as Equation (3.15) shows, the noise transfer function is now a second-order high pass function. Thus, the signal to noise ratio at low frequencies is higher than in a first-order modulator. This concept, called the cascaded modulator or the MASH modulator, MASH modulators of any order are unconditionally stable if individual modulators comprising the MASH are stable. In this case, the individual modulators are first-order ones, and thus always stable. Hence, the order of the MASH modulator can be increased at will without causing any stability problems.

4. System Design:

Based on theoretical analysis shown in sections two and three, a GaussianFSK transmitter in UHF band by direct modulation of ΣΔ modulator fractional-N synthesizer will be designed for the following requirements :

- Frequency range:869.9 MHz– 900.4 MHz
- Channel spacing:500kHz
- Data rate:150kb/s
- Frequency deviation : 300kHz
- Phase noise:less than -84dbc/Hz@10 kHz

The sigma delta modulator will be used to implement the system since it has the following properties:

- Eliminating spurious digitally.
- Allowing good phase noise performance.

The sigma delta modulator's type in this system is MASH modulator contains three stages of accumulator. The GFSK is selected to provide high spectral efficiency. The frequency deviation is set by the following equation [7]:

Freq. deviation = $(F_{crystal} * 2^m)/(R * 2^{14})$

Where R represents reference division, $F_{crystal}$ represents crystal frequency and m represents modulation control. Figure (7) shows the schematic diagram of the system. **ADF7012** chip contains reference divider, MASH modulator, and phase frequency detector.

The loop filter is a passive 3rd order filter which is selected in the system because it has the following properties

- The least complex loop filter.
- Smallest resistor thermal noise.
- Maximum resistance to variation of VCO gain & PFD gain.

For this system, R1= 1.84k, R2=3.77k, C1= 35.5 PF, C2= 483 PF and C3 = 11.2 PF.

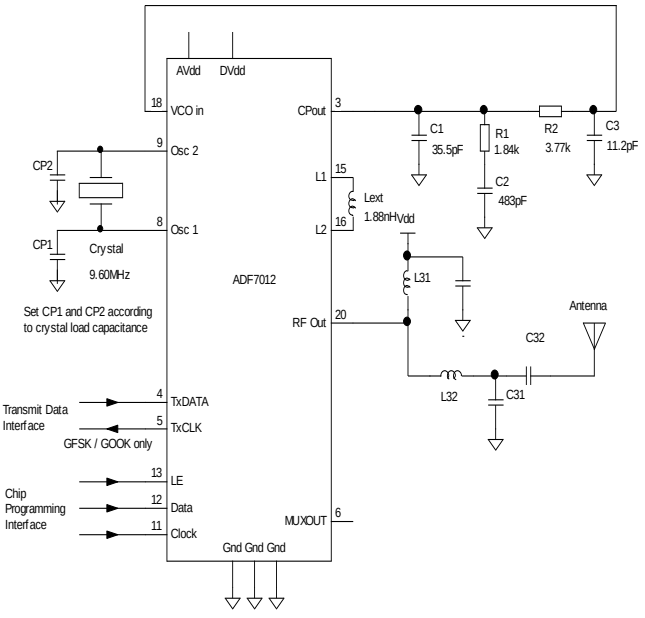

Fig. 7. Schematic Diagram of the System.

5. Results of Simulation:

A system is simulated by ADI SRDLsim version 1 software & we obtain the following results:

1. Single frequency simulation of transmitter: Figure (8) shows block diagram of test configration for the transmitter:

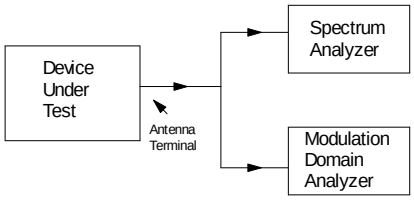

Fig. 8. Block Diagram of Test Configuration.

From this test , the following results of single frequency 900MHz and span 1MHz of spectrum analyzer are obtained and shown in figures (9) and (10).

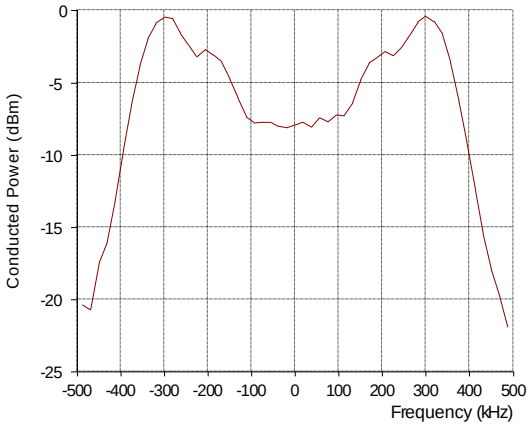

Fig.9. Spectrum Analysis of Single Frequency 900 MHz Transmitter with Span 1MHz.

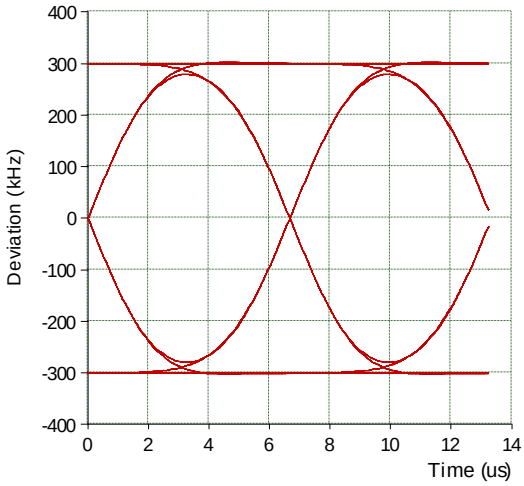

Fig.10. Modulation Domain Analysis of GFSK Transmitter at Frequency 900 MHz.

2. Phase noise: it is the most critical parameter which describes short term frequency instability include fluctuations in signal's phase or frequency that less than 1sec. This is shown in figure (11).

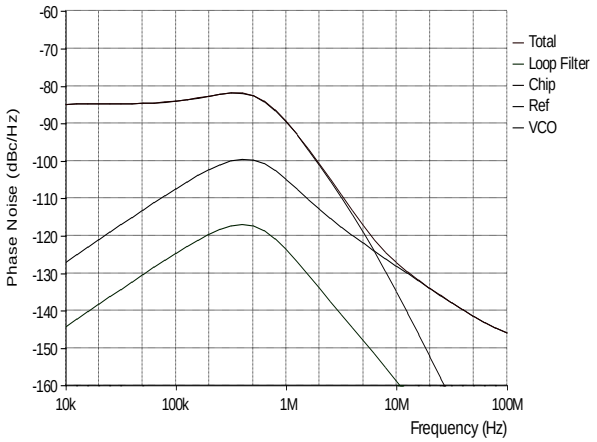

Fig.11. Phase Noise of Fractional Synthesizer.

3. Settling time: it is defined as the time needed for switching the synthesizer from one frequency to another. The settling time of our synthesizer is less than 2μsec for frequency switching (870-890) MHz as shown in Figure (12).

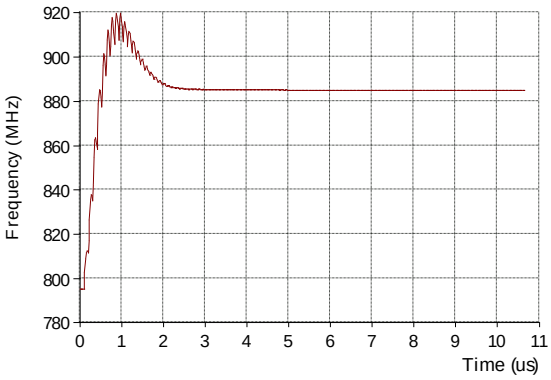

Fig.12. Settling Time.

6. Discussion and Conclusions:

The UHF GFSK transmitter has been presented by direct modulation of fractional synthesizer. The simulation results of this transmitter achieve the following specifications:

- Frequency range:869.9 MHz–900.4 MHz
- Channel spacing : 500kHz
- Data rate : 150kb/s
- Frequency deviation : 300kHz
- Phase noise:less than -84dbc/Hz @10 kHz

The system is proposed in this research that allows fractional-N frequency synthesizers to be directly modulated at low data rates while simultaneously achieving good noise performance. The technique allows digital phase/frequency modulation to be achieved without mixers or D/A converters in the modulation path. The resulting transmitter design is primarily digital in nature and reduced to its fundamental components—a frequency synthesizer that accurately sets the output frequency, and a Gaussian filter that provides good spectral efficiency.

Among various techniques, the ΣΔ-modulator fractional-N synthesizer has been selected to provide direct modulation of transmitter since it has several advantages:

- Low feedback –divider ratio results in lower phase noise with fine step size.
- Low phase noise contributions are lowered by 20log (L), where L is the fractional modulus.
- Larger loop B.W. results in lower lock time.

The direct modulation method by fractional synthesizer is preferred on traditional methods of transmission because it provides the following benefits:

- Low power consumption.
- Low cost.
- Small size.

7. References:

[1] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," in *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 186–7, 1995.

[2] T. A. Riley and M. A. Copeland, "A simplified continuous phase modulator technique,"*IEEE Transactions on Circuits and Systems — II: Analog and Digital Signal Processing*, vol. 41, no. 5, pp. 321–328, May 1994.

[3] Goldberg, Bar-Giora., "Digital frequency synthesis demystified",1999.

[4] J.A Crawford, "Frequency synthesizer Design Handbook", Artech house, Norwood, 1994.

[5] Dean banerjee "PLL performance , simulation & design" 4th edition, 2005.

[6] Li Lin, "Design Techniques for High Performance Integrated Frequency Synthesizers for Multi-standard Wireless Communication Applications" UNIVERSITY OF CALIFORNIA, Ph.D., thesis, 2000.

[7] The Analog device series Data sheet, 2004.

[8] W. Djen and P. Shah, "Implementation of a 900 MHz transmitter system using highly imtegrated ASIC," in *IEEE 44th Vehicular Technology Conference*, pp. 1341–5 vol. 2, June 1994.

[9] Lascari lance, "Accurate phase noise prediction in PLL frequency synthesizers" Applied Microwave & Wireless, VOL. 12, No.5, May 2000.

[10] I. A. Koullias, J. H. Havens, I. G. Post, and P. E. Bronner, "A 900 MHz transceiver chip set for dual-mode cellular radio mobile terminals", in *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 140–1, Feb. 1993.

تصميم ومحاكاة Gaussian FSK مرسلة باستعمال مركب ترددات من نوع ΣΔ Modulator Fractional-N

علي محمد نوري
قسم هندسة المعلومات والاتصالات/كلية هندسة الخوارزمي/جامعة بغداد

الخلاصة

يهدف البحث الى تصميم ومحاكاة GaussianFSK مرسلة باستعمال مركب ترددات من نوع (ΣΔ modulator fractional-N وبالمواصفات التالية: مدى الترددات الخارجة (869.9 – 900.4) ميكا هرتز، نسبة تدفق المعلومات (150kb/s)، مدى الفصل بين القنوات (500kHz)، زمن تحويل 1 مايكرو ثانية ومستوى ضوضاء طوري (85-) ديسبيل عند 10000 هرتز من التردد الخارج. تقنيات الدوائر الحديثة ساهمت بشكل فاعل في زيادة التكامل للمرسلات والمستلمات لاشارات الراديو. خواص مثل قلة استبداد القدرة، صغر الحجم و قلة الكلفة هي التي تعتبر المقياس الخاص بالتصميم والتي من خلالها يتم الحكم على اداء النظام. ان التضمين المباشر بواسطة مركب الترددات من نوع ΣΔ (Fractional - N) تم اقتراحه في هذا البحث وذلك لان هذه الطريقة تؤمن الخواص التي نحتاجها مثل قلة استبداد القدرة وصغر الحجم وقلة الكلفة. عملية التضمين من نوع ΣΔ وضعت في دورة قفل الطور الرقمي للسيطرة على القيمة الكسرية لمقسم التردد وبواسطته يتم ازالة الطفيليات مع مستوى طفيليات اقل ومستوى ضوضاء طوري جيد. نوع التضمين (Gaussian FSK) الذي تم استخدامه للحصول على كفاءة طيفية عالية في الاشارة المضمنة. ان التطبيقات لهذه المرسلة هي قلة كلفة نقل المعلومات اللاسلكي، انظمة الامان، السيطرة عن بعد بواسطة اشارات (RF) والعداد اللاسلكي.