Practical Results of a Five-level Flying Capacitor Inverter

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Abstract

This paper investigates the realization of a five-level Flying Capacitor Inverter. After a brief description of general Power Electronic Converters and an introduction to the advantages of Multilevel Inverters over conventional two-level Inverters the main focus is on the five-level Flying Capacitor Inverter. The Flying Capacitor Multilevel Inverter (FCMI) is a Multilevel Inverter (MI) where the capacitor voltage can be balanced using only a control strategy for any number of levels. After a general description of five-level FCMI topology, the simulation and experimental results are presented. The capacitor voltage is stabilized here with various output voltage amplitude values. The simulation and experimental results of five-level FCMI show that the voltage is stabilized on capacitors using the control strategy. A single-phase five-level FCMI model is currently being developed and constructed in the laboratory. Some of the experimental results are available.

Keywords: multilevel inverters, control strategy, IGBT, DCMI, FCMI, active power filters, unified power flow controller.

1 Introduction

Since the 1990s switching devices such as GTO thyristors and IGBT transistors have been widely used in Power Electronic Converters. These Converters are currently classified into:

a) Rectifiers — Converters that convert an input alternating voltage and current into output direct voltage and current;

b) Inverters — Converters that convert input direct voltage and current into output alternating voltage and current;

c) DC voltage Converters (Choppers) — Converters that convert input direct voltage and current of one value into output direct voltage and current of other values;

d) AC Converters — Converters that convert input energy with one parameters (alternating voltage, current, number of phases, frequency) into alternating output energy with other parameters.

This paper investigates the realization of a Multilevel Inverter (MI) that belongs to category (b) — Inverters.

The conventional single-phase Inverter generates ordinary rectangular voltage on its output. Power Electronic switchers are switched to two input voltages — positive and negative. This type of Inverter is called a two-level Inverter. Electronic Switchers are stressed by full input DC voltage in this case. The Electronic Switcher voltage stress can be reduced using a series connection or a Multilevel Inverter.

Conventional Inverters are used in low-voltage electrical equipment up to 1 kV.

For medium and high voltage equipment over 1 kV, a series connection of GTO/IGBT or a Multilevel Inverter is applied. The three-level Inverter is the Multilevel Inverter with the smallest number of levels. The advantages of three-level Inverter topology over conventional two-level topology are:

- The voltage across the switches is only one half of the DC source voltage;
- The switching frequency can be reduced for the same switching losses;
- The higher output current harmonics are reduced by the same switching frequency.

Multilevel Inverters find applications in new areas of medium- and high- voltage applications, e.g. frequency Inverters for high voltage adjustable speed drives, Inverters for high- voltage compensators, high- voltage Unified Power Flow Controllers (UPFC), and high- voltage Active Power filters, etc.

Voltage sources of the next levels can be realized as separated sources or as voltage capacitor dividers. Separated sources require further Power Hardware. The chief problem in Multilevel Inverters with capacitor dividers is the proper control strategy for voltage stabilization without additional Power Hardware.

The most popular types of MI are Diode Clamped Multilevel Inverters (DCMI) and Flying Capacitor Multilevel Inverters (FCMI). For a three-level topology, only both types of MI can be designed without any separated voltage sources or auxiliary Power circuits. Papers [6] and [7] compare these two types of Multilevel Inverters from various points of view. The comparison was realized for the same output Powers. The mathematical models for both types of In-

verters were investigated in the Simulink program. This comparison showed that three-level DCMI requires the total capacity of all capacitors to be at least two times lower than three-level FCMI in order to achieve the same capacitor voltage swinging. Hence the DCMI solution is considered more effective for three-level MI.

However, for a higher number of levels than 3 in DCMI, the capacitor voltage cannot be balanced using only the control strategy. Additional circuits or independent sources are required. For example, paper [3] describes the stabilization of capacitor voltage in five-level DCMI using the advanced strategy together with auxiliary circuits. On the contrary the voltage can be stabilized using only the control strategy in FCMI for all levels.

Multilevel Inverters with more than three levels are mainly used in high-voltage applications for the voltage greater than 10 kV.

The purpose of this paper is to present the results of a theoretical study and the practical realization of a five-level FCMI. After a brief description of five-level FCMI topology, we present the simulation and experimental results. The simulation and experimental results of five-level FCMI are carried out on a model, supplied with 200 V DC source. Both of these results show that a five-level output voltage is generated and the capacitor voltage is stabilized using only the control strategy. Five-level FCMI is investigated here because only this strategy is able to balance the capacitor voltage using only the control strategy.

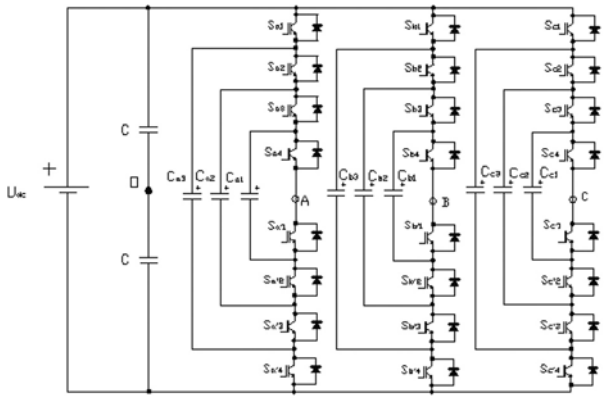

Fig. 1: Scheme of the three-phase five-level Flying Capacitor Inverter

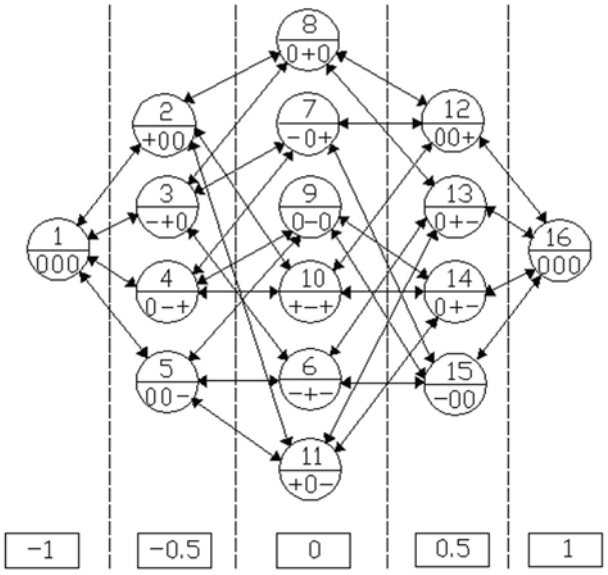

Fig. 2: Switching states in the five-level FCMI

2 Five-level flying capacitor topology simulation

2.1 Description of five-level FCMI topology

Generally, FCMI with N levels needs $N-2$ flying capacitors for each phase. The scheme of a three-phase five-level Flying Capacitor Inverter is shown in Fig. 1. This Figure shows $(5-2)\times 3 = 9$ capacitors. The lower levels on phase outputs A, B, C are achieved as the difference between supply voltage U_{dc} and capacitor voltages $U_{c1,2,3}$.

The idea of the control strategy can be explained using Fig. 2. This Figure shows the possible switching states for one phase of five-level FCMI. The voltage levels are signed (-1), (-0.5), (0), (0.5), (1) and these numbers represent the relation between the voltage levels and the DC supply voltage $+ = (1)$ and $- = (-1)$. Each level can be obtained by one or more switching states. The number of possible states is represented by the number of circles in the corresponding level. The upper number in the circle is the switching state number. The lower three signs represent the voltage behaviour on the corresponding capacitors: increasing $(+)$, decreasing $(-)$, or unchanging (0). The rectangles on the bottom show the output voltage value in relative units that correspond to each column of the states. This behaviour is correct for positive output current polarity. The bidirectional bonds show the possible state transitions between levels that fulfil the condition that only one couple of IGBTs can switch in one moment (one of them ON, the other one OFF). The five-level Inverter allows sixteen possible states.

All four upper switches (Fig. 1) are ON in state 16; consequently, the output voltage is $+1$, equal to one half of the DC voltage source $U_{out} = U_{dc}/2$.

At states 12, 13, 14, 15, the output voltage is the difference between one half of the DC voltage source and any capacitor voltages with the resulting out-

put voltage 0.5. Different capacitors are connected for specific states. In these states, the three upper switches are one lower switch ON and the others are OFF. Which actual switchers are ON and OFF depends on actual switching state.

In states 6, 7, 8, 9, 10, 11, the output voltage is the difference between the half DC voltage source and any capacitor voltages. The resulting output voltage is 0. In these states, two upper switches are and two lower switches are ON. Similarly as in the previous states, the specific switchers which are ON and OFF depends on concrete switching state.

In states 2, 3, 4, 5, one upper switch and three lower switches are ON, and all the rest are OFF. The output voltage is the difference between one half of the DC voltage source and any capacitor voltages. The result is -0.5.

In the state 1, all four lower switches (Fig. 1) are ON; consequently, the output voltage is -1, equal to one half of the DC voltage source $U_{out} = U_{dc}/2$.

In state 1, the four lower switches are ON, and the four upper switches are OFF. The output voltage is equal to the negative DC voltage source $U_{out} = -1$.

The transition of the switching states to the next state is implemented to ensure the capacitor voltage balance. This is determined by the polarities of all three capacitor voltages and also the output current polarity. The switching state in the five-level FCMI in Fig. 2 is shown only for positive output current polarity. The full matrix of switching states transition, including all capacitor voltages and the current polarity would require a large table, and cannot be published in this paper.

All the flying capacitor values in each phase are accepted the same $C_1 = C_2 = C_3 = C$. The dividing capacitor voltages are defined in the following equations: (1) defines the voltage on capacitor C_1, (2) defines the voltage on capacitor C_2 and (3) defines the voltage on capacitor C_3.

$$U_{c1} = \frac{3}{4} \times U_{dc} \tag{1}$$

$$U_{c2} = \frac{1}{2} \times U_{dc} \tag{2}$$

$$U_{c3} = \frac{1}{4} \times U_{dc} \tag{3}$$

2.2 Load simulation

The behavior of this Inverter was simulated for a passive load using MATLAB Simulink only for one phase. The connection of a three-phase passive load is depicted in Fig. 3. The passive load in this picture is represented by series connection of resistance R and reactance ωL in each phase in star connection. The output voltage phasors $U_{outA}, U_{outB}, U_{outC}$ can represent line-to-zero voltages to zero point of source O_S or zero point of load O_L. The real model was realized only for one phase, and therefore the phasors represent line-to-zero point of source voltages. They are shifted at an angle of $-\frac{2}{3} \times \pi$ from each other. The direction of the output current is shown in Fig. 3 only for phase A.

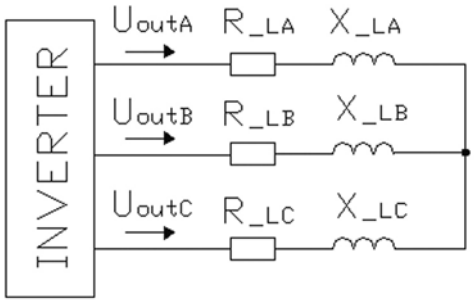

Fig. 3: Scheme of a three-phase equivalent inverter with a passive load

The voltage equation for a one-phase model can be written according to the second Kirhgoff law (see Equation (4)).

$$\hat{U}_{outA} = \hat{I}_{outA} \times (R_A + j\omega \times L_A) \tag{4}$$

This connection allows us to change the load type from pure resistive to pure inductive by changing the values of resistance R_A or L_A. If inductance $L_A \approx 0$ and the resistance has any definite value, the load is pure resistive and the output current is in the phase with the output voltage and has the same shape as the voltage. If the inductance has a definite value and the resistance is close to zero, the load is purely inductive and the first harmonic of the current is 90° delayed to the first harmonic of the voltage. If the reactance is equal to the resistance, then the first harmonic of the current is 45° delayed to the first harmonic of the voltage.

2.3 Simulation strategy

The input parameters of the five-level FCMI for the Simulink program are given in Table 1. The Inverter is supplied from a 200 V DC source, the flying capacitor values of C_{A1}, C_{A2}, C_{A3} are identical and are equal to 1 000 μF. The load values are: $R_A = 150\ \Omega$, $\omega L_A = 110\ \Omega$.

The equations for the variable input parameters used in the Simulink program are given in Table 2. They are: angular frequency omega, load inductance L and load impedance Z. Initial capacitor voltages U_{c1}, U_{c2}, U_{c3} are taken from equations (1)–(3).

Fig. 4 shows the simulation results from Simulink with output voltage U_{out}, output current I_{out}, and capacitor voltages U_{c1}, U_{c2}, U_{c3}. Flying capacitor voltages fluctuate around their initial values: $U_{c1} = 3/4U_{dc} = 150$ V, $U_{c2} = 1/2U_{dc} = 100$ V, $U_{c3} = 1/4U_{dc} = 50$ V.

Table 1: Parameter values for the Matlab Simulink program in five-level FCMI

$f = 50$	network frequency, [Hz]
$N = 14$	switching triangular carrier frequency per period, [number/period]
$X = 110$	reactance, [Ω]
$R = 150$	resistance, [Ω]
$C = 0.001$	clamping capacitor, [F]
$R_c = 0.001$	resistance of capacitor circuit, [Ω]
$U_{dc} = 200$	direct voltage source, [V]
$U_{max} = 0.95$	amplitude of output voltage, [p.u.]

Table 2: Variable input parameter equations used for the Matlab Simulink program in five-level FCMI

$\Omega = 2 \cdot \pi \cdot f$	angular frequency
$L = x/\Omega$	inductance
$Z = \sqrt{RR + XX}$	impedance
$U_{c01} = 3/4Udc$	initial voltage on the capacitor C_1
$U_{c02} = 1/2Udc$	initial voltage on the capacitor C_2
$U_{c03} = 1/4Udc$	initial voltage on the capacitor C_3

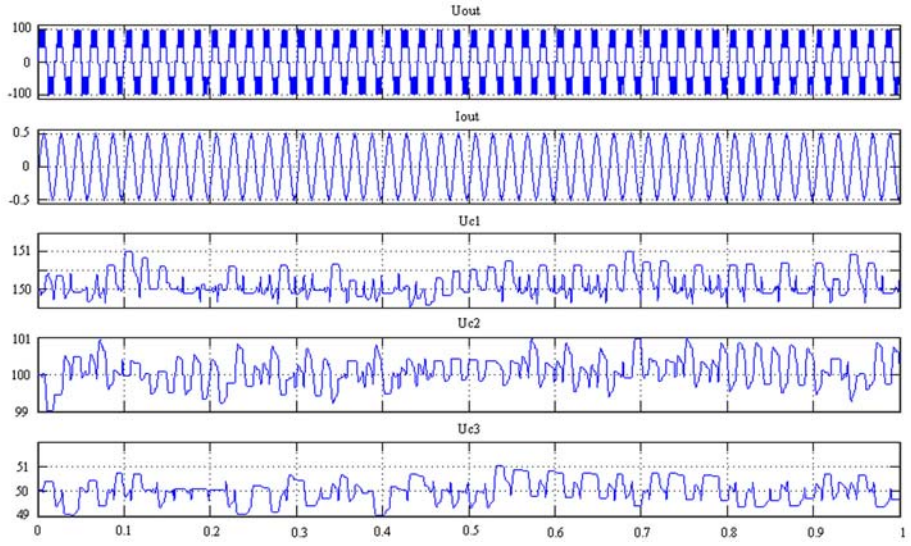

Fig. 4: Output voltage U_{out}, output current I_{out} and flying capacitor voltages U_{c1}, U_{c2} and U_{c3} of five-level FCMI with a resistive inductive load

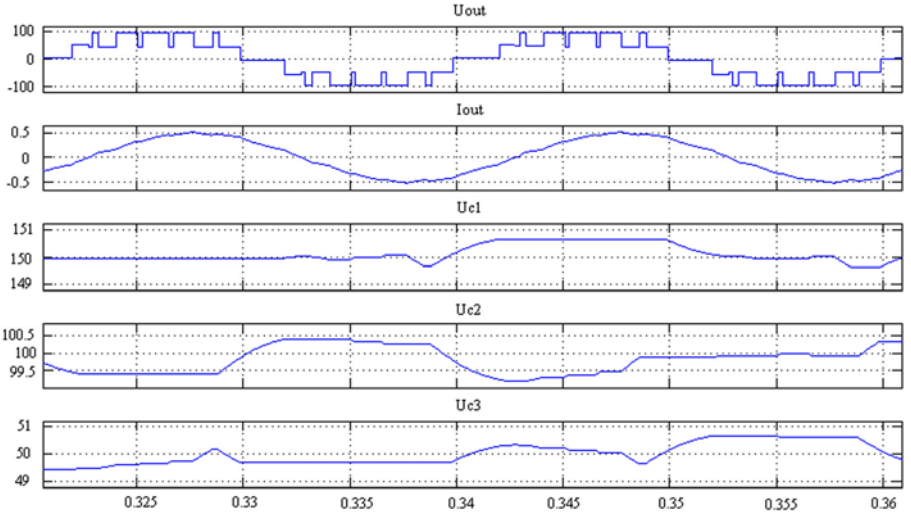

Fig. 5: A zoom-in of output voltage U_{out}, output current I_{out} and capacitor voltages U_{c1}, U_{c2}, U_{c3} shown in Fig. 4

Fig. 5 gives a close look into the results in Fig. 4. Five-level output voltage is obtained, the output current is shifted around 45° against the first harmonic of output voltage, and its shape is close to sinusoidal. The flying capacitor voltages are stabilized without any independent sources or additional circuits.

3 Realization of a five-level flying capacitor inverter

3.1 Structural schemes

The one-phase five-level FCMI with a DC source 30...200 V experimental equipment is in operation in the laboratory of the Department of Electric Drives and Traction at CTU. The main purpose is to achieve the necessary experimental results with the generated five-level output voltage U_{out} and capacitor voltages stabilized. The principal scheme of the Power part of the one-phase five-level FCMI is shown in Fig. 6. The IGBT switch modules are chosen as main switching elements of IRG4BC20KD type, including an International Rectifier anti-parallel diode (http://www.irf.com). The value of each capacitor is $C_1 = C_2 = C_3 = C = 1\,000\ \mu$F and the voltage in each capacitor is distributed as shown in Equations (1)–(3). The type of load can be selected as resistive or inductive. The scheme includes Measurement, Drive and Protection, dSPACE BOARD, and Power circuit.

The structural scheme of the experimental model has been proposed and also constructed. Fig. 7 shows the control conception of IGBT drivers and its connection to capacitors C_1, C_2, C_3, load A, all control boards, all power supplies and dSPACE.

The IGBT driver protects the IGBT in the event of over-current. It is constructed in four floors, each floor having two drivers: right and left. Each driver is supplied from a 15 V voltage source that is supplied from 230 V network and converted to 15 V in the output.

The Drive and Protection board ensures galvanic separation between dSPACE BOARD and IGBT driver. It also provides protection for IGBT. When at least one of IGBT indicates over-current, it switches off all the IGBTs and indicates which of them is out of order.

The measurement part measures the capacitor voltage and the load current, and converts the actual values into logic voltage signals compatible with input of dSPACE.

Fig. 8 shows some details of the experiment prototype — the IGBT drivers, the power supplies, the flying capacitors, the input capacitors and the drive and protection board. Some of the boards are constructed as printed circuits, some are soldered in wires. All the boards are interconnected with wires.

The schemes of the voltage capacitor and the load current measurement, the IGBT drivers, the drive and protection board, and pictures of the other devices will be published in the final thesis.

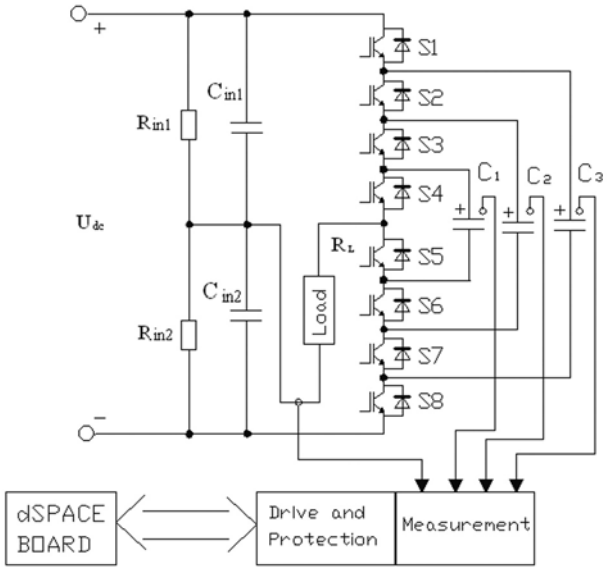

Fig. 6: Principal scheme of the single-phase five-level flying capacitor inverter that is in the laboratory

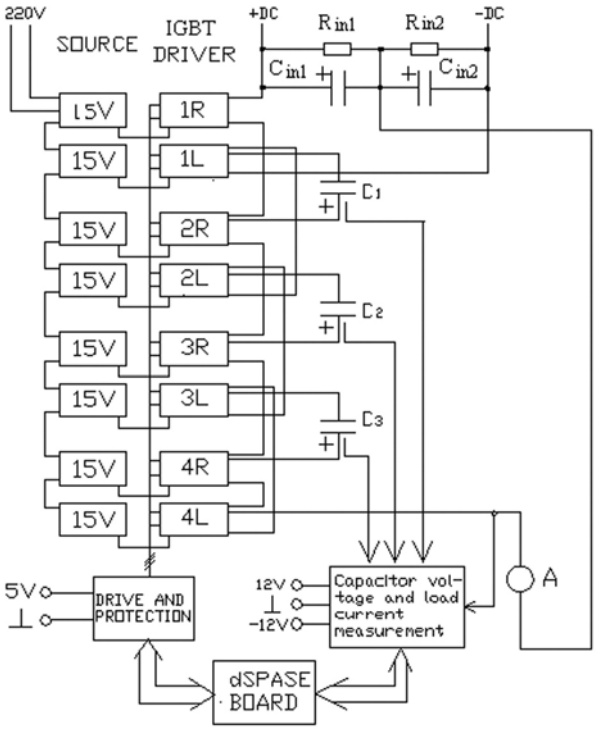

Fig. 7: Structural scheme of the experimental model of a single-phase five-level flying capacitor inverter

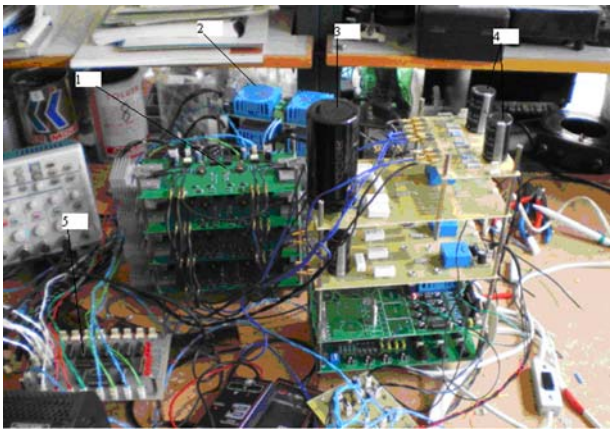

Fig. 8: Pictures of some experimental prototype details: 1 – IGBT drivers; 2 – Power Supplies 15 V; 3 – flying capacitor C_1; 4 – input capacitors; 5 – drive and protection board

3.2 Experimental results

The parameters of the five-level FCMI for experimental measurements are given in Table 3. The control is realized using the MATLAB Simulink program, and also with the same parameters as in the simulation measurement. Only the first three parameters from Table 3 are controlled in dPSACE. They are: output frequency f, switching triangular carrier frequency per period N, and control amplitude output voltage U_{max}.

Table 3: Parameter values for the Matlab Simulink program in five-level FCMI for experiment results

$f = 50$	network frequency, [Hz]
$N = 14$	switching triangular carrier frequency per period, [number/period]
$U_{max} = 0.6 \ldots 0.95$	amplitude of output voltage, [p.u.]
$X = 110$	reactance, [Ω]
$R = 150$	resistance, [Ω]
$U_{dc} = 200$	direct voltage source, [V]

The other parameters, e.g. direct voltage source U_{dc}, resistance R_A, inductance L_A, capacities C_1, C_2, C_3, are realized physically in laboratory conditions.

Output voltage U_{out} is the control parameter, and it is set in relative units. The maximum value must be a little less than 1, so that it can be modulated.

Fig. 9 shows experimental results for output voltage U_{out} and output current I_{out} with control amplitude output voltage $U_{max} = 0.95$. Five-level output voltage is generated. It is in the scale 5 V per division and the voltage probe has the divider in oscilloscope 1/20. The voltage axis with its values is on the left. Its amplitude is around ±100 V. The output current has a curved shape close to sinusoidal and its delay to the first harmonic voltage is around 45° because the load is resistive inductive. The scale of the current is 5 mV per division and its probe divider is 10 mV/A. The current axis is on the left. The current amplitude is ±0.5 A.

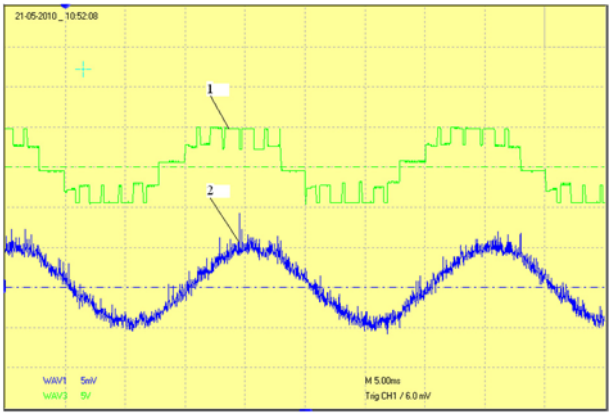

Fig. 9: Experimental results: 1 – output voltage U_{out}; 2 – output current I_{out} with $U_{max} = 0.95$

Fig. 10 shows the experimental results for output voltage U_{out} and output current I_{out} with control amplitude output voltage equal to $U_{max} = 0.6$. The generated five-level output voltage U_{out} has much narrower pulses than the corresponding voltage in the previous case. The output current amplitude is almost two times lower than the previous amplitude corresponding to an output voltage value of U_{out}.

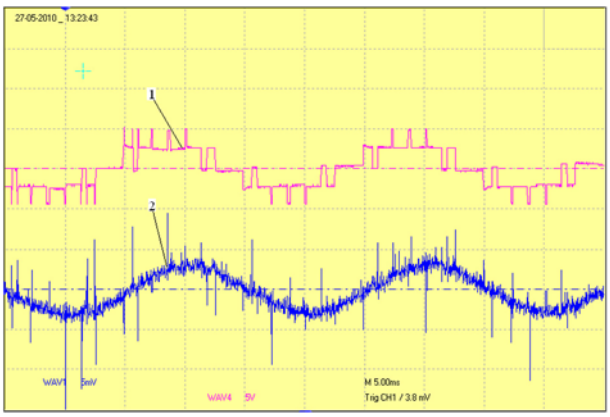

Fig. 10: Experimental results: 1 – output voltage U_{out}; 2 – output current I_{out} with $U_{max} = 0.6$

Fig. 11 shows the experimental results for capacitor voltages U_{c1}, U_{c2}, U_{c3} measurement with $U_{max} = 0.95$. They are all stabilized same as in the simulation results above the same value. Voltages U_{c1} is stabilized above a value of 150 V, U_{c2} is stabilized above a value of 100 V and U_{c3} is stabilized above 50 V, which corresponds with equations (1), (2) and (3).

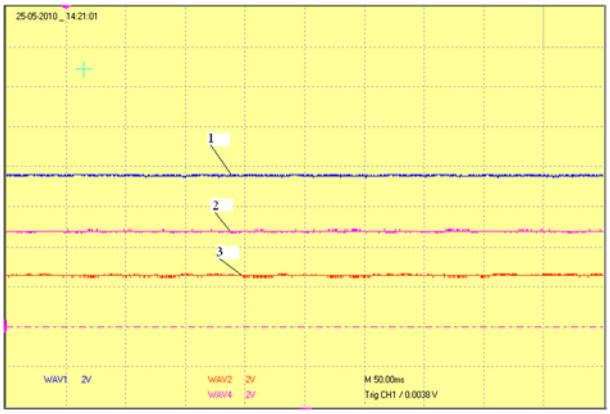

Fig. 11: Experimental results of flying capacitor voltages: 1 – U_{c1}, 2 – U_{c2}, 3 – U_{c3} with $U_{max} = 0.95$

Fig. 12 shows the experimental results of capacitor voltages U_{c1}, U_{c2}, U_{c3} with the control amplitude output voltage $U_{max} = 0.6$. The capacitor voltages are all stabilized at the same values as with the control amplitude output voltage $U_{max} = 0.95$ (Fig. 11).

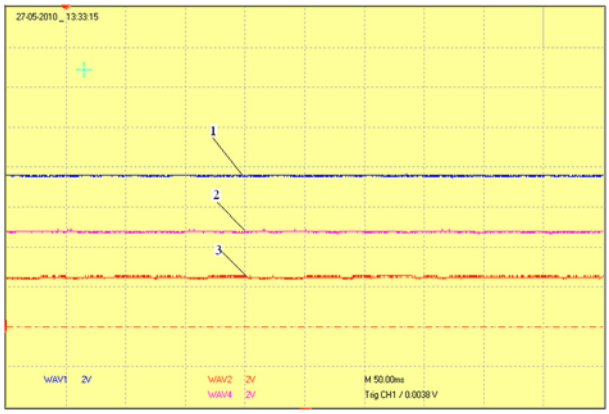

Fig. 12: Experimental results of flying capacitor voltages: 1 – U_{c1}, 2 – U_{c2}, 3 – U_{c3} with $U_{max} = 0.6$

4 Conclusion

A brief description of a five-level FCMI inverter has been presented. The principle of five-level FCMI function has been presented. A simulation model of the Inverter with its passive load has been designed and tested. The capacitor voltage in the five-level FCMI has been balanced without auxiliary circuits. Five-level FCMI is practically investigated because the capacitor voltage is balanced here using only the control strategy. The simulation results are confirmed by experimental results realized in five-level FCMI. The five-level output voltage is generated and the capacitor voltages are stabilized using the selected control strategy. The experimental measurements are presented for two different control output voltage amplitudes U_{max}, and in both cases the capacitor voltages are stabilized.

Acknowledgement

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