Communication between a Matrix Converter Modulator and a Superset Regulator

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This work deals with the modulator of a matrix converter and its communication with the superset regulator. A switching algorithm is briefly introduced. The input voltage measurement method is presented. In the last part of the paper, the testing of communication between the superset regulator and the modulator in FPGA technology are also presented.

Keywords: matrix converter, FPGA, VHDL, power electronics.

1 Matrix converter

A matrix converter is a direct frequency changer. This converter consists of an array of n×m bidirectional switches arranged so that any of the output lines of the converter can be connected to any of the input lines.

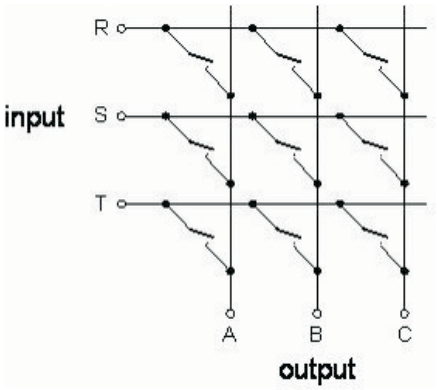


Fig. 1: Matrix converter 3×3

The bidirectional switch is realized by using some semiconductor devices. They can be either discrete or integrated to the module. The bidirectional switch can be implemented in various ways. For the matrix converter, we chose modules which include 3 bidirectional switches in common emitter a configuration. The modulator is thus realized for these switchers.

2 Switching

Two basic conditions must be kept during switching:

- The converter is supplied by three-phase system voltage sources. The input must therefore not be short-circuited, which means that every output phase is connected with not more then one input phase.
- An inductive load is premised. Disconnection would lead to overvoltage, and for this reason the output circuit cannot be interrupted during routine running.

It is important to choose an efficient switching algorithm. For the modulator we chose four-step switching driven by the input voltage. For this method it is necessary to know the polarity of the voltage between the input lines. The advantage of this algorithm is its simplicity and the fact that it can be driven even by low current values. The disadvantage is longer commutation time. The processes of four-step switching driven by input voltage are insinuated in tables Table 1. and Table 2. We can see that it is possible to use the same switching algorithm for different current direction. The modulation algorithms can therefore be driven only by the input voltage.

3 Modulation strategy

Indirect Space Vector Modulation (ISVM) is used in the matrix converter. We can imagine the matrix converter as an indirect converter with a virtual DC link. We can therefore use some processes well known from classical indirect frequency converters.

It is necessary to ensure the right timing for command switching and to generate the guard delay and then the switching at the right moments. We achieve this by adding or subtracting the given times of the switching combinations and comparing them with the values of saw courses, Fig. 2.

Using the proper switching combinations, the necessary rate of switching IGBT during one switching period can be reduced. The process of achieving a different order of switching in even and odd periods is presented on Fig. 2 and Fig. 3.

4 Communication

Switching commands and times of switching combinations are sent from the superset regulator per PC 104 bus. All PC 104 bus signals are identical in definition and function to their ISA counterparts [4]. Signals are assigned in the same order as on the edgecard connectors of ISA, but transformed to the connector pins.

The matrix converter modulator was programmed in VHDL language, and consists of several parts. First part provides the right switching signals for IGBTs, and puts the guard delay between the separate switching steps. The second part generates switching commands at the right time. Other

Table 1: Algorithm for four-step switching driven by the input voltage for a bidirectional switch with a common emitter for $U_{RS} > 0$ and $I_A > 0$

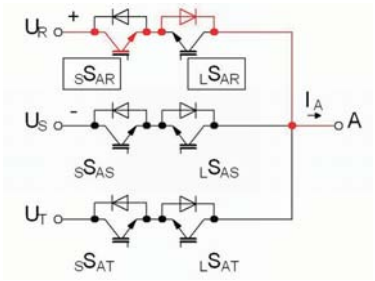
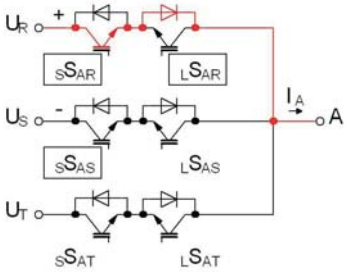
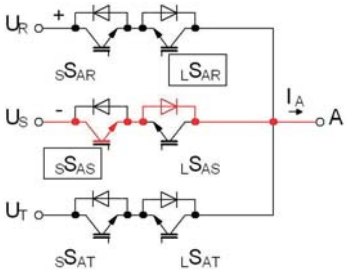
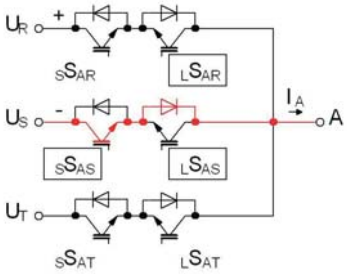
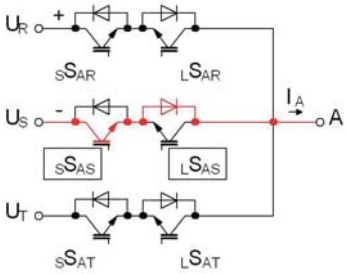
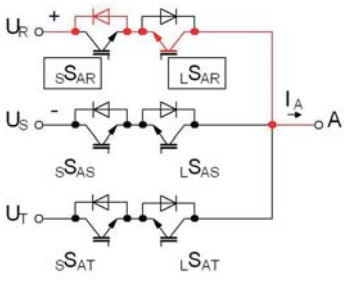
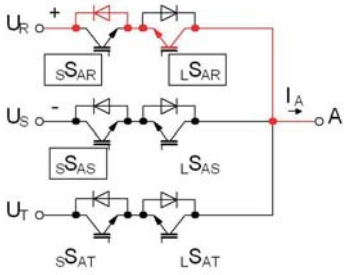
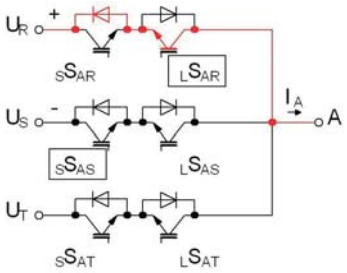
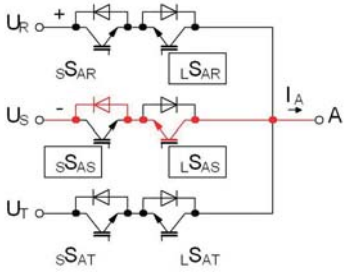
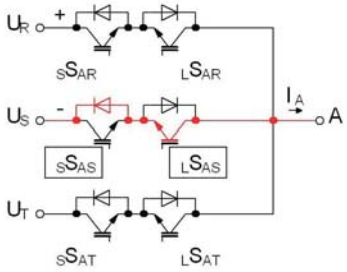
$U_{RS} > 0$ & $I_A > 0$		
		Initial State
		First Step
	Hard Switching	Second Step
		Third Step
		Fourth Step

Table 2: Algorithm for four-step switching driven by the input voltage for a bidirectional switch with a common emitter for $U_{RS} > 0$ and $I_A < 0$

$U_{RS} > 0$ & $I_A < 0$		
		Initial State
		First Step
		Second Step
	Soft Switching	Third Step
		Fourth Step

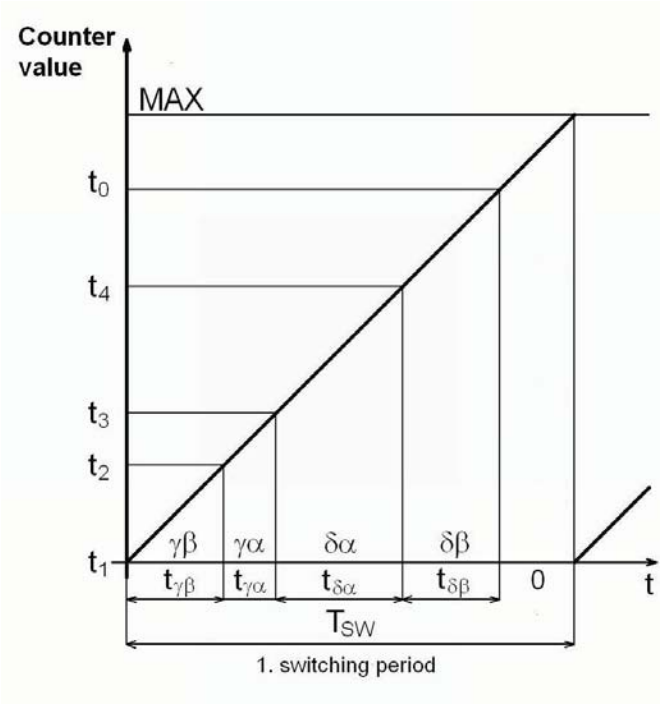


Fig. 2: Acquiring of the right timing for a switching command (odd period)

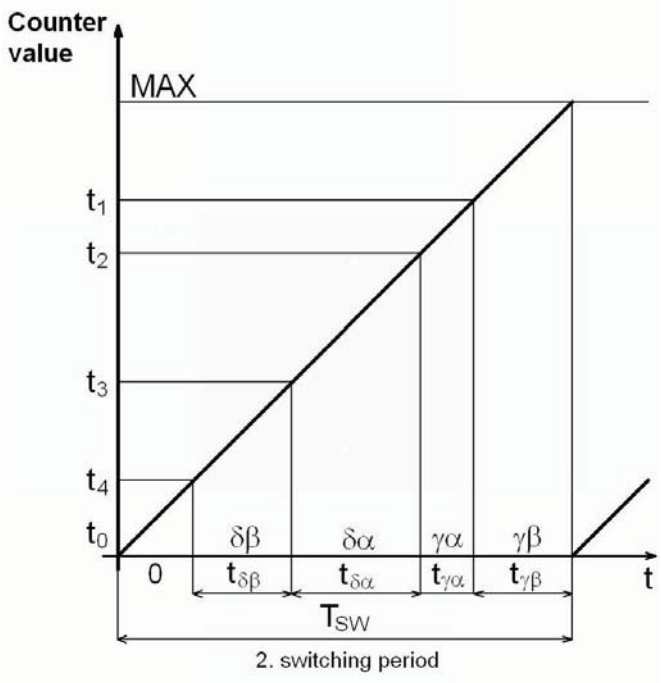


Fig. 3: Acquiring of the points of optimized switching (even period)

parts provide communication. Several registers are realized in FPGA and each of them has its own address. Some registers are "read only", some are "write only", and some are "read and write". There is one state register which is cleared after it is read by the regulator. The information about the state of hhe modulator and the values from the A/D converters can be read due to the superset regulator.

The regulator can write to the modulator switching the command and times of switching combination.

The Modulator has a mode register which changes its function. This is necessary for testing this modulator and for the possibility of changing the HW of superset regulator.

5 Regulator

The superset regulator is a one-desk PC from RTD or Kontron with the PC 104 bus. During the test of communication test, we found that the one-desk Kontron PC read from the PC 104 bus in 16-bit mode, in a way different from that described in the universal bus specification. When we want to read 16-bit from PC 104 bus, we have to read only the even addresses. Because a one-desk Kontron PC reads first from the even address and than from address +1, which is an odd address. Special bus handling has to be implemented for this onedesk PC. The setting of this bus handling is enabled by the mode register.

The functions of a one-desk PC are the same as those of other PCs. The difference between these two kinds of PCs is in their size. A one desk PC, as the name indicates, is realized on a single PCB (90.17 mm × 95.89 mm). AS a matter interest, a one-desk RTD PC has a standard operating temperature from –40 °C to +85 °C.

An advantage of using a PC as a superset regulator is its high-computing power in floating-point arithmetic and the possibility of using of high-level language. A disadvantage of this solution is the need for real-time programming on a device which is not primary specified for this. Another problem is with high-speed input and output. This problem must be solved in each case, because DSP (standard used as a regulator) has only 12 PWM outputs and a 3×3 matrix converter needs 18 outputs. When we realize the modulator in FPGA, each high speed input and output and some algorithms can by replaced for this technology. This means that the superset regulator has more time for regulation algorithms and for communicating with the user. This is an important advantage for development, especially at a university, where students do not have a lot of time for a detailed study of DSP architecture.

6 Analog-digital converters

FPGA can control analog-digital converters (ADC), evaluate signals from IGBTs drivers and detect errors and control relays in power circuits. All acquisition of these values is very simple for a superset regulator, because it is only a read or a write operation to a specific address in memory via the PC104 bus.

There are 4 sigma-delta ADCs and 4 Voltage Frequency ADCs on the board with the FPGA circuit.

These converters are served in FPGA, using RAM memory. The outputs from these two kinds of ADC are serial data. The number of ones in all the data sent per measured period is equal to the average value. The data is put into the shift register and the number of ones can easily be determine by adding the input data and subtracting the output data. Then appropriate register directly has an average value with an accurately defined delay. A disadvantage is the relatively long delay. Another feature of this evaluation is that the ADC values are filtered. This is an advantage when we pass thorough zero. However higher frequencies cannot be measured.

7 Communication testing

A special program has been developed in C language for testing communication. This program writes values to the registers realized in FPGA. These values are changed in the FPGA circuit by a defined process, and then they are read from the superset regulator. A program placed in the superset regulator controls the values from the registers, and if it finds a mistake it notifies the error.

This program was later modified for testing analogdigital converters and IGBT drivers. The testing program is not in real-time, but it speed is sufficient for measurements on the FPGA board. The testing program allows the measured value be saved to the RAM superset regulator and, after this program is closed, to the flash memory. The measured values can be processed in MS Excel or Matlab to graphic form.

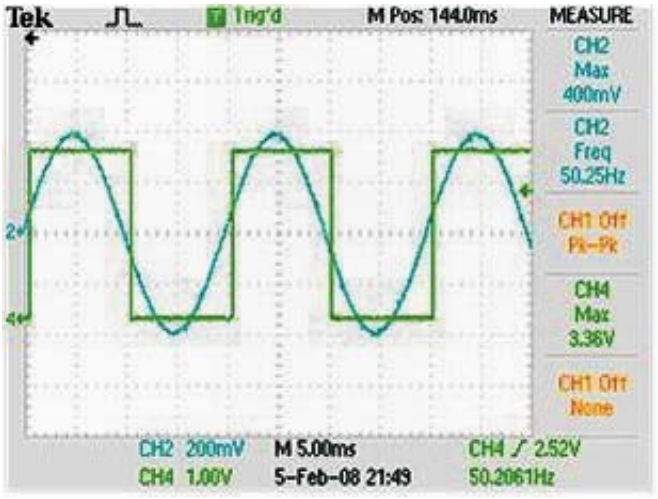


Fig. 4: Input signal to the ADC and evaluation polarity

Fig. 4 presents the input signal to the ADC and the most significant bit from the FPGA register which contains the measured value. This bit represents the polarity. The delay measure is equal to the shift between this signal and the input to the ADC. Fig. 5 presents the values measured by ADC. We can see that the measured value corresponds to the input signal.

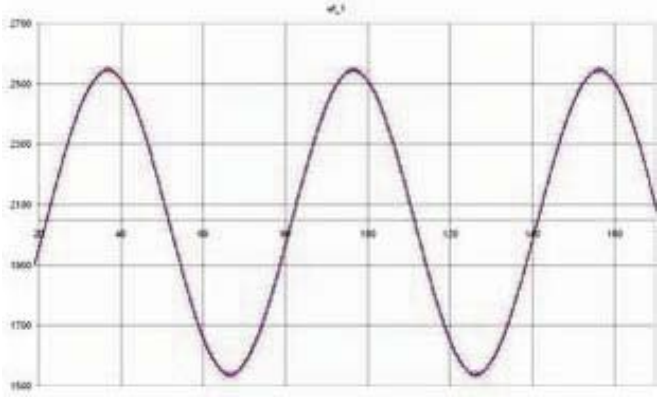


Fig. 5. Values measured by ADC on FPGA board

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