An Integrated Simulation Method for Built-in Test System Based on Stateflow

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To satisfy the application requirements of built-in test (BIT) technology in equipment design for testability and prognostic and health management (PHM), an integrated simulation method for BIT system based on stateflow is proposed. Based on the analysis of the operating modes of BIT system, an integrated simulation principle of BIT system is given. Main simulation elements, such as fault-interference superposition insertion, fault detection and fault isolation, are analyzed with their stateflow models established. The integrated modeling and simulation process of BIT system is presented, and a design flow of an integrated simulation insertion data set is given. Finally the BIT system of a typical avionics power board is applied to the integrated simulation method, and simulation results are used to evaluate the capabilities of fault detection, fault isolation and false alarm rejection of the BIT system.

1. Introduction

Built-in test (BIT) (Luo et al., 2011) is an automatic test capability of fault detection and location (Correia Da Silva et al., 2009). BIT plays an important role in improving the diagnosis capability and the prognostic and health management (PHM) level of a system. The technologies of false alarm rejection (Tian et al., 2011), simulation verification and evaluation (Tong et al., 2008) are the research focuses of BIT.

Dependency model (Shi et al., 2012a) can be used to simulate and verify BIT system, with diagnosis strategies (Sun et al., 2007) and testability quantitative evaluation results (Liu et al., 2011) generated. Interference and false alarm rejection cannot be modeled by the dependency model, but they can be modeled by electronic design automation (EDA) (Shi et al., 2011). The modeling and simulation process of EDA is much more complicated. Stateflow which is based on the concepts of finite state machine theory, flowcharting and state transition symbols can make up for the above shortcomings of the dynamic simulation of fault transition (Lv et al., 2010).

Some researchers have established the models of fault insertion, interference insertion, fault detection and false alarm rejection for power-on BIT (POBIT) system (Shi et al., 2012b) and periodic BIT (PBIT) system (Li et al., 2012) separately. There is a lack of an integrated simulation method considering fault-interference superposition insertion, fault detection and fault isolation for a BIT system which is made of several kinds of BITs. This paper proposes an integrated simulation method for BIT system based on stateflow, and the capabilities of fault detection, fault isolation and false alarm rejection of the BIT system can be evaluated by simulation results.

2. BIT system operating modes and integrated simulation principle

2.1 BIT system operating mode analysis

The test result of BIT can be denoted by a binary model. If a test is passed, the result of the test is denoted as "0", otherwise the result is denoted as "1". Because of interference, BIT may raise false alarms which will lead to unnecessary maintenance, so some false alarm rejection measures should be taken to improve the BIT performance.

BIT mainly has three operating modes: power-on mode, periodic mode and maintenance mode. They are described as follows:

- Power-on mode: when a system is powered on, a specified test is launched until a fault is detected or the test is finished.
- Periodic mode: during the operation of a system, a specified test is launched at regular intervals.
- Maintenance mode: when a system task is finished, a specified test is launched for maintenance, inspection and check.

BITs of power-on mode, periodic mode and maintenance mode are called POBIT, PBIT and maintenance BIT (MBIT) respectively. In power-on mode, POBITs operate and output detection results. When the power-on mode is over, BIT system switches to the periodic mode and PBITs output detection results regularly. Both of the results of POBITs and PBITs are stored in MBIT, and detailed BIT information can be reviewed in the maintenance mode.

2.2 BIT system integrated simulation principle

The integrated simulation principle of BIT system is shown in Figure.1. Based on the analysis of the BIT system operating modes, simulation elements of each operating mode can be determined. Then the stateflow models of the simulation elements can be established to constitute an integrated simulation model of the BIT system in the Matalb/Simulink environment. Finally simulations can be carried out by inserting a fault, an interference or both into the BIT system, and simulation results can be used to calculate the values of fault detection rate (FDR), fault isolation rate (FIR) and false alarm rate (FAR) to evaluate the capabilities of fault detection, fault isolation and false alarm rejection.
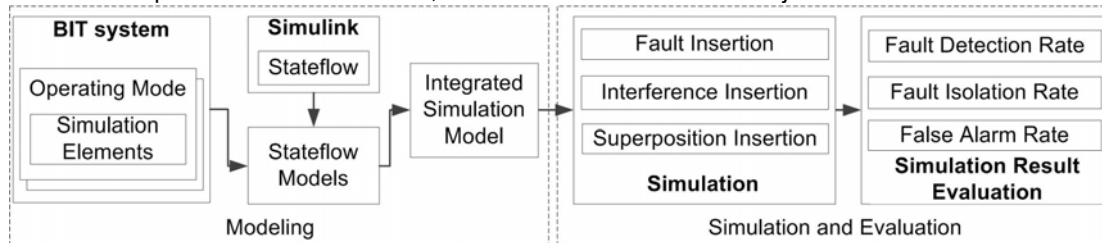

Figure 1: Integrated simulation principle of BIT system based on stateflow

3. Main simulation elements and their models

The main simulation elements of BIT system contain fault insertion, interference insertion, fault detection, fault isolation, false alarm rejection and so on. The stateflow models of fault insertion, interference insertion and false alarm rejection are the same as those established by Shi et al. (2012b) and Li et al. (2012). The stateflow models of fault-interference superposition insertion, fault detection and fault isolation should be established for the integrated simulation.

(1) Fault-interference superposition insertion model

Fault-interference superposition state is the state of a UUT (unit under test) which is faulty and also influenced by interference, and the superposition can result in either normal state or remained faulty state. Fault-interference superposition insertion can be accomplished by inserting a fault and an interference simultaneously. As shown in Figure. 2, the output of the state_model is sent to the input of the interference_model, and the fault state and the interference state can be superposed in the interference model. The output value of the superposition is the sum of state output value and interference value.

(a) Fault-interference superposition   (b) Inner of interference model
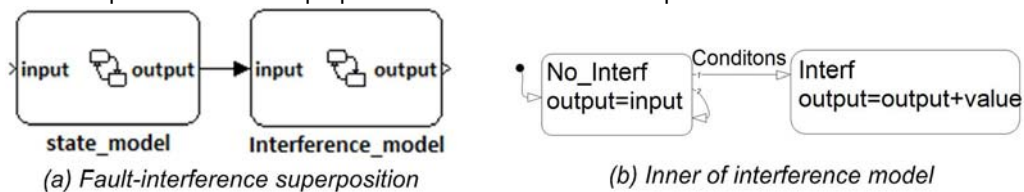
Figure 2: Fault-interference superposition insertion model

(2) Fault detection model

Fault detection model is used to determine if a test signal is in threshold, as shown in Figure. 3. In power-on mode (t<=T), POBIT which doesn't consider interference outputs "1" directly if the BIT signal is not in threshold. In periodic mode (t>T), PBIT which considers interference needs repetitive judgements for false alarm rejection, and a result is output after tested for more than *tn* times.
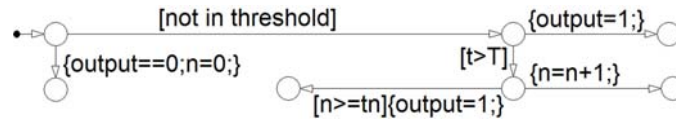
Figure 3: Fault detection stateflow model

(3) Fault isolation model

Fault isolation model is used to locate a fault which has been detected by the fault detection model. All BIT outputs can be encoded in a truthtable in order to determine the faulty unit of a UUT. As shown in Figure. 4, BIT1 and BIT2 are encoded in the truthtable. The encoded result o1 shows the occurrence of a fault, and the encoded result o2 shows the code of the fault. Both o1 and o2 can be sent to a display model which shows all fault diagnosis information. The encoded POBIT results are output at the end of power-on mode (from t1 to t2), and the encoded PBIT results are output at regular intervals in periodic mode (t>t2).

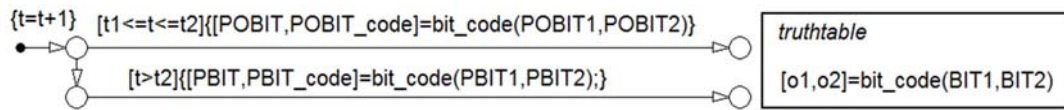Figure 4: Fault isolation stateflow model

4. The integrated modeling and simulation of BIT system

4.1 Integrated modeling

The integrated modeling flow of BIT system is similar to the modeling flow of POBIT system (Shi et al., 2012b), which mainly includes achieving BIT design materials, analyzing testability requirements, determining simulation elements and establishing BIT simulation model four steps. This paper focuses on the integrated modeling of POBIT and PBIT, and the following aspects should be further analyzed: a) the modeling of the operating modes and their switch way, and b) the modeling of fault-interference superposition insertion, fault detection and fault isolation. Based on the above analyses, an integrated simulation model can be established by integrating the stateflow models of POBIT and PBIT.

4.2 Integrated simulation

The integrated simulation flow of BIT system is also similar to the simulation flow of POBIT system (Shi et al., 2012b), which mainly includes establishing an insertion data set of BIT simulation, selecting an insertion item, running a simulation and achieving an output data set of the simulation four steps. The insertion data set of the integrated simulation should contain both the fault insertion in power-on mode and the fault-interference superposition insertion in periodic mode. As shown in Figure. 5, the improved design flow of an insertion data set is as follows:

a) If a fault insertion is needed according to a simulation task, get the insertion information of the fault; otherwise, go to the next step.

b) If an interference insertion is needed according to the simulation task, get the insertion information of the interference; otherwise, go to the next step.

c) Generate an insertion item by combining the fault insertion information and the interference insertion information.

d) If all insertions are parsed and their information is gotten, combine all insertion items and establish an insertion data set of the integrated simulation of BIT system; otherwise, return to step a).
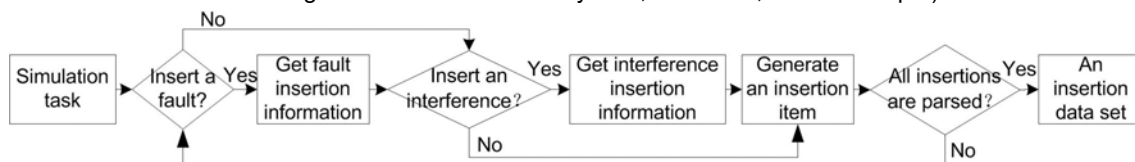

Figure 5: Design flow of an insertion data set of integrated simulation

With an insertion item of the insertion data set input into the integrated simulation model, a simulation can be run. Using the simulation output data of all insertion items, FDR, FIR and FAR can be calculated to evaluate the BIT system.

5. Case study

5.1 Case description
The BIT system of a typical avionics power board is applied to the proposed integrated simulation method based on stateflow. The power board consists of a central alarm power module (CAM), a ground alarm power module (GAM) and an integrated alarm power module (IAM). Fault modes, interferences and BITs of the power board are shown in Table. 1.

Table 1: Fault modes, interferences and BITs

Module	Fault mode	Fault No.	Interference (Interf)	Interf No.	BIT
CAM	CAM voltage (C_Volt) fault	1	C_Volt_Interf	1	C_Volt_BIT
	CAM current (C_Curr) fault	2	C_Curr_Interf	2	C_Curr_BIT
	CAM temperature (C_Temp) fault	3	C_Temp_Interf	3	C_Temp_BIT
GAM	GAM voltage (G_Volt) fault	4	G_Volt_ Interf	4	G_Volt_BIT
	GAM current (G_Curr) fault	5	G_Curr_Interf	5	G_Curr_BIT
	GAM temperature (G_Temp) fault	6	G_Temp_Interf	6	G_Temp_BIT
IAM	IAM voltage (I_Volt) fault	7	I_Volt_Interf	7	I_Volt_BIT
	IAM current (I_Curr) fault	8	I_Curr_Interf	8	I_Curr_BIT
	IAM temperature (I_Temp) fault	9	I_Temp_Interf	9	I_Temp_BIT

The voltage BITs and the current BITs have two modes: power-on mode and periodic mode, while the temperature BITs have only periodic mode.

5.2 Integrated modeling
As shown in Figure. 6, the integrated model of the BIT system of the power board consists of a state model, an interference model, a BIT detection model, a BIT code model and a display model.
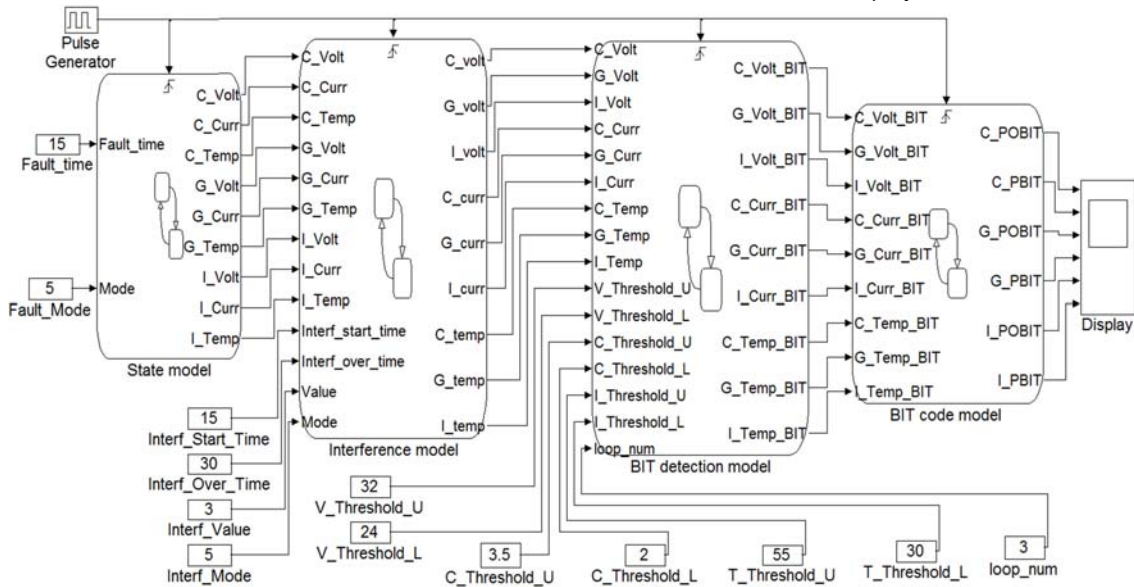

Figure 6: Integrated simulation model of power board BIT system

The state model includes a normal state and nine fault states. In the normal state, voltage, current and temperature of three modules are in the thresholds [V_Threshold_L, V_Threshold_U], [C_Threshold_L, C_Threshold_U] and [T_Threshold_L, T_Threshold_U] respectively. The nine fault states correspond to the nine fault modes in Table. 1. The interference model includes the nine interferences in Table. 1. If an interference is inserted, the interference value (Interf_Value) is superposed to the output value of the state model, which may result in the change of the state. The BIT detection model is made of the nine BITs in Table. 1 and the detection models of two BITs are shown in Figure. 7. The temperature BIT has only periodic mode. The voltage BIT which has power-on mode and periodic mode needs an additional mode judgement step: if the BIT is in power-on mode (t<=10), a result is output directly; or the result should be tested for loop_num times before output. As shown in Figure. 8, the BITs of each module are encoded in the truthtable. CAM_POBIT and CAM_POBIT_CODE, the encoded results of C_Volt_BIT, C_Curr_BIT

and C_Temp_BIT in power-on mode, indicate the occurrence and the code of CAM fault at the end of the power-on mode (9<t<10). CAM_PBIT and CAM_PBIT_CODE, the encoded results of C_Volt_BIT, C_Curr_BIT and C_Temp_BIT in periodic mode, indicate the occurrence and the code of CAM fault regularly when t>10. The encoding processes of other modules are similar to that of CAM. All encoded results are sent to the display model, and faulty units can be determined according to the displayed information.
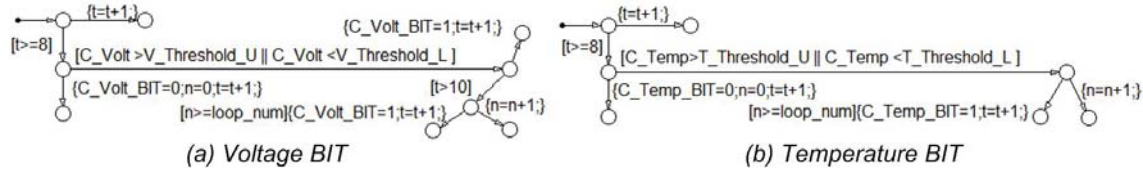

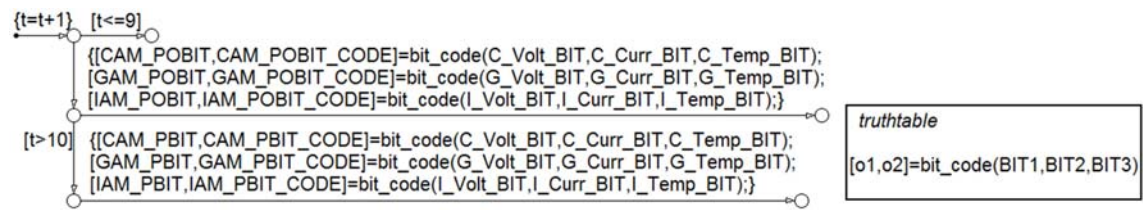*Figure 7: Two BIT detection models*

Figure 8: BIT code model

5.3 Integrated simulation

The insertion data set of the integrated simulation of the power board BIT system is shown in Table. 2. The parameter settings of the integrated model are shown in Table. 3. A rising edge trigger pulse with an amplitude of 1 and a period of 1 s was given before the integrated simulation. An insertion item was selected from the insertion data set and input into the integrated model for every simulation. The simulation results of all insertion items and the judgements of the simulation results are listed in Table. 4.

Table 2: Insertion data set of the integrated simulation of the power board BIT system

Item No.	Fault Insertion			Interference (Interf) Insertion				
	Fault name	Fault No.	Insertion time (s)	Interf name	Interf No.	Interf value	Interf start time (s)	Interf over time (s)
1	C_Volt fault	1	5	—	—	—	—	—
2	G_Volt fault	4	15	—	—	—	—	—
3	—	—	—	C_Curr_Interf	2	5	20	25
4	—	—	—	G_Temp_Interf	6	20	12	15
5	G_Curr fault	5	15	G_Curr_Interf	5	3	15	30
6	C_Curr fault	2	5	C_Curr_Interf	2	3	15	20
7	I_Curr fault	8	18	I_Curr_Interf	8	3	18	20
8	G_Temp fault	6	15	C_Temp_Interf	3	12	17	25
9	I_Temp fault	9	12	G_Volt_Interf	4	10	20	22

Table 3: Parameter settings of integrated model

Voltage Threshold	Current Threshold	Temperature Threshold	Test Number	Simulation Time
[24, 32]	[2, 3.5]	[30, 55]	3	30 s

Table 4: Simulation results and judgements

Item No.	1	2	3	4	5	6	7	8	9
Simulation Results	CAM Fault	GAM Fault	CAM Fault	Normal	Normal	CAM Fault	IAM Fault	GAM Fault	CAM Fault	IAM Fault
Result Judgements	CD	CD	FA	CD	UD	CD	CD	CD	FA	CD

Where, CD indicates a detection is correct; FA indicates a false alarm; UD indicates a fault is not detected.

6. Results analysis

The simulation results of Table. 4 were determined by observing the curves in the display model. Compared to Item 1, only PBIT raised an alarm for Item 2, which resulted from the different insertion times. The CAM_PBIT raised a false alarm for Item 3 because of C_Curr_Interf. For Item 5, G_Curr_Interf was superposed onto G_Curr fault, and the deviation between G_Curr fault state and the normal state was eliminated. C_Curr_Interf of Item 6 existed for a period of time, CAM_PBIT raised an alarm when C_Curr_Interf was cancelled. For Item 8, G_Temp fault and C_Temp_Interf were inserted into different modules, and CAM_PBIT raised a false alarm because of C_Temp_Interf. The existence time of the interferences of Item 4, 7 and 9 were short enough and false alarm rejection measures eliminated the influences of the interferences. Based on the above analyses, G_Curr_BIT and C_Temp_BIT were suggested increasing the repetitive test number so that false alarms can be further eliminated.

Using the results of Table. 4, the evaluation parameters of the power board BIT system were calculated and shown in Table. 5.

Table 5: Evaluation parameter calculation results

Inserted Fault Number	Correctly Detected Fault Number	Correctly Isolated Fault Number	Total Number of Detected Faults	False Alarm Number	FDR	FIR	FAR
7	6	6	8	2	85.7 %	100 %	25 %

7. Conclusions

BIT system can be used to detect and isolate faults of a UUT. Most BIT systems are made of several kinds of BITs. Based on the stateflow modeling tool and the analysis of the operating modes of BIT system, this paper proposes an integrated modeling and simulation method for BIT system, which can accomplish the dynamic simulation of fault transition and contribute to a feasible method for evaluating BIT system. As space is limited, only a set of typical insertion data is designed to illustrate the proposed method. The integrated model doesn't consider the cross-links among faults and the situation of multiple fault insertion and multiple interference insertion, which need to be completed in future research.

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