Electronic Communications of the EASST Volume 080 (2021)



Conference on Networked Systems 2021 (NetSys 2021)

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4 pages

Guest Editors: Andreas Blenk, Mathias Fischer, Stefan Fischer, Horst Hellbrueck, Oliver Hohlfeld, Andreas Kassler, Koojana Kuladinithi, Winfried Lamersdorf, Olaf Landsiedel, Andreas Timm-Giel, Alexey Vinel ECEASST Home Page: http://www.easst.org/eceasst/ ISSN 1863-2122



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Abstract: Molecular communication (MC) is a new paradigm for communication processes with a variety of applications such as health care and industrial sectors. The rapid development of MC, with the support of testbeds and simulators, requires scalable modeling tools. In this paper, we propose a field-programmable gate array (FPGA) design-based approach for the emission, diffusion, and reception of molecules. Results exhibit a close correspondence to state of the art analytical modeling of MC processes.

Keywords: Molecular communication, FPGA, nanotechnology, nanodevices.

1 Introduction

Molecular communication (MC) systems is nowadays a focus of study due to their promising applications in health care and communication industry sectors [KDB⁺19,HSF⁺19]. Supporting them, a variety of simulators have been developed to account for the emission, diffusion, and reception processes; examples include nanoNS3, BiNS2c, AcCoRDc as discussed in [BD19]. Also, a field-programmable gate array (FPGA)-based approach for gain and delay simulation using Verilog has been proposed in [SSLP20]; yet, without exploiting all simulation capabilities. In a different direction, in this paper, we concentrate on the physical MC model suggested in [PA10]. The given transfer functions of the model can be transformed into the discrete model and, in turn, be directly implemented on FPGA hardware. The resulting implementation allows better simulation speed thanks to the parallel structure of the FPGA and the flexibility to quickly adapt the test framework. The contribution of this paper is to provide a proof of concept, showing that scalable MC modeling is possible in FPGA technology.

2 Modeling MC Channels in FPGA

Following the report in [PA10], a MC system is represented by processes of molecules emission, diffusion, and reception, as depicted in Figure 1. These subsystems, when characterized through their equivalent transfer functions as linear time-invariant systems (LTI) system (cf. Equations (1) to (3) [PA10]), can be then conceived in FPGA technology. To that end, departing from these equations, we follow the transformation process described in Figure 2a to devise their corresponding FPGA block diagram [OS13]. In a first step, we apply the bilinear transform on the continuous transfer function H(s) to derive the discrete counterpart H(z). In a second step, we extract the coefficients a_i and b_i from H(z) to devise an FPGA block diagram in a direct form II, as shown in Figure 2b. Finally, in a third step, we implement the system through a direct form II structure [OS13].

During the **emission process**, the particles are being released into the communication medium, depicted as space S, or taken back into the reservoir E from it. The particles emission process converts the input signal $s_T(t)$ into particles concentration $r_T(t)$ as shown in Figure 1. In the transfer function this behavior is



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Figure 1: MC channel abstraction, inspired by [PA10].

expressed trough the resistor value as $R_e = 1/D$ (cf. Equation (1)). The capacitance $C_e = 1$ F is a constant as consequence of balancing the net flux of emitted particles.

$$H_A(s) = \frac{1}{1 + sR_eC_e} \qquad (1) \qquad H_B(s) = K_0(\|\bar{x}\|\sqrt{s^2 + s\beta}) \quad (2) \qquad H_C(s) = \frac{sC_r}{1 + sR_rC_r} \qquad (3)$$

The diffusion process allows for the particles to travel through the medium by converting the particle concentration $r_T(t)$ at the emitter to the particle concentration $c_R(t)$ at the receiver (cf. Figure 1). It is modeled as an LTI system through the channel impulse response (CIR) function given in [PA10, Eq. 24]. The resulting transfer function is shown in Equation (2), where $K_0(x)$ is a second kind modified Bessel function, $\|\bar{x}\|$ is the distance from the transmitter to the receiver, $\beta = \frac{1}{c_d \cdot \tau_d}$, $c_d = \pm \sqrt{D/\tau_d}$ is the wave-front speed, and τ_d is the relaxation time. This transfer function is however not a rational function, which prevents the immediate application of



(a) Methodology to derive the(b) Generalized block diagram in Direct form Direct form II block diagram. II.

Figure 2: Deriving the direct form II block diagram

the methodology mentioned above. To circumvent this problem, we approximate the Bessel function in Equation (2) using curve fitting in MatLab to derive rational functions for the absolute values. Then, we depart from a standard rational function with a numerator of second-degree and a denominator of third-degree to apply the methodology depicted in Figure 2.

Finally, the **reception process** converts the given concentration $c_R(t)$ into the output signal $s_R(t)$ (cf. Figure 1). The receiver R consists out of receptors, which can capture a particle or release the captured



	Channel		Transmitter		Receiver $N = 20$		Receiver $N = 100$	
Coefficients								
i	a_i	b_i	a_i	b_i	a_i	b_i	a_i	b_i
0	1	-0,0417	1	5e-11	1	8e7	1	9,52e7
1	3,1120	0,0410	1	5e-11	0,6	-8e7	0,9048	-9,52e7
2	-3,2228	0,0417						
3	1,1108	-0,0410						
Analytical solution								
a_1	None		-	$-\frac{T-2R_eC_e}{T+2R_eC_e}$	$-rac{T-2R_rC_r}{T+2R_rC_r}$			
b_0	None			$\frac{T}{T+2R_eC_e}$	$\frac{2C_r}{T+2R_rC_r}$			
b_1	None			$\frac{T}{T+2R_eC_e}$	$-\frac{2C_r}{T+2R_rC_r}$			

Table 1: The coefficients of the nominator (b_i) and denominator (a_i) after the bilinear transformation and analytical solutions

particle back. These are modeled to capture the particle only when it is not currently occupied, and it will only release the particle back whenever it was occupied by the particle. An electrical output signal is produced by a particle (ligand) forming a receptor-ligand complex, which is represented as a particle capturing. The rate constant *k* controls how hard it is for a molecule to form and break a receptor-ligand complex, hence $R_r = 1/k$, and the number of receptors is controlled through the capacitance C_r .

Based on the transfer functions in Equations (1) and (3), we obtain the analytical solutions in Table 1, based on which we evaluate the coefficients. Through these coefficients, we then directly implement the FPGA scheme depicted in Figure 2b. In the case of Equation (2), we derive the scheme's coefficients after their approximation.

3 Results

In this section, we compare the derived FPGA design to the original model in [PA10]. Selected results depicted in Figure 3 have been obtained through MatLab and Simulink. Parameters are taken from [PA10] for the emitter, the diffusion, and the reception processes. Thus, emitter and the diffusion transfer functions are depicted in the frequency spectrum from 0–1 kHz, while the receiver in the range 0–10 MHz. The normalized gain of the transmitter module in Figure 3(a) is depicted considering $D = 10^{-6} \text{ m/s}^2$, $C_e = 1 \text{ F}$, and $R_e = 1/D$ at a sampling frequency of 10 kHz. The normalized gain of the diffusion module in Figure 3(b) is obtained for the distance $\|\bar{x}\| = 10 \,\mu\text{m}$, relaxation time $\tau_d = 10^{-9} \text{ s}$ at a sampling frequency of 2.5 kHz. The normalized gain of the receiver module shown in Figure 3(c) is obtained for rate constant $k = 10^8 / \text{M/sec}$, with a variable number of receptors of $C_r = 20 \text{ F}$ and $C_r = 100 \text{ F}$, $R_r = 1/k [\Omega]$ at a sampling frequency of 10 MHz.

The corresponding coefficient values and analytical solutions for them are shown in Table 1 in the respective columns. Results exhibit that the FPGA design repeats the original transfer function. Transmitter and emitter modules show results, which are not equal but quite identical to the results obtained through the LTI system model. In the diffusion module, due to the fact that we approximated the function's absolute values, their resulting discrete representation exhibits some differences. Nevertheless, the result remains quite accurate up to about 800 Hz.

4 Conclusions

The resulting FPGA design of a MC model is supposed to scale well with thanks to parallelism. Scalable desings can be conceived as simply as connecting more direct form II blocks (cf. Figure 2 b). Besides, the complexity of the system model will be directly given by the total of adders and multipliers used on the same block. The communication testbed could potentially run multiple communication systems simultaneously with each system modeling a different parameters setup. The suggested design is generic, meaning it is not fixed to any concrete implementation, thus, it can be applied in any FPGA





Figure 3: Comparison of FPGA simulations and modelled transfer functions.

technology. As a future improvement, a more flexible or even analytical solution could be found. Another possible improvement is related to the design, which can be extended to multiple communication lines to model a complex multiple-input and multiple-output (MIMO) systems.

Acknowledgements: Reported research was supported in part by the project *MAMOKO* funded by the German Federal Ministry of Education and Research (BMBF) under grant number 16KIS0917.

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