

A Gain Programmable Analog Divider Circuit Based on a Data Converter

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Abstract—Analog dividers are widely used in analog systems. Analog realization of such circuits suffer from limited dynamic range and non-linearity issues, therefore, extra circuitry should be required to compensate these types of shortcomings. In this paper a gain controllable, analog divider is proposed based on data converters. Our circuit can be implemented both in current and voltage mode by selecting proper architectures. The resolution, power consumption and operation speed can be controlled by proper selecting of components. Another advantage of our circuit is its gain programmability. Moreover, the gain can be adjusted independently based on the relationship between input signals. Our proposed method offers two different gain control abilities, one for situation that the numerator signal is bigger than the denominator, and another gain is applied when the denominator is larger than the numerator. As a result, no extra amplifier is required for signal amplification. Moreover, the input and output signal nature can be chosen arbitrarily in this circuit, i.e. input signal may be a voltage signal while the output signal is current. Simulation results from SPICE confirm the proper operation of the circuit.

Keywords—analog divider; data converter based divider; gain adjustable analog divider; wide dynamic range analog divider; mixed signal divider

I. INTRODUCTION

Dividers are a basic building block in analog signal processing systems. Such a system usually requires high precision dividers to realize modulators, squarers, automatic level controllers, etc. Several techniques are proposed in the literature to design dividers in continuous time monolithic circuits from different technologies. CMOS dividers are reported both in the strong and weak inversion. Strong inversion approaches are very complex in signal interfacing point of view [1-7]. On the other hand, weak inversion circuits are slow [8-13]. Some researchers design dividers working in voltage mode, while current mode circuits can achieve lower power consumption, higher dynamic range and linearity. An alternative approach is using switched capacitor technique [14]. Authors in [15] proposed a novel method of realization of voltage mode analog multiplier/divider based on the modified cyclic data converter. A current mode multiplier/divider in

current mode utilizing data converter techniques is presented in [7]. In this paper, a novel divider circuit is proposed based on data converters. There is a trade-off between speed, power consumption and resolution that can be managed by properly selecting the components used. Furthermore, our proposed circuit can produce the output signal with controllable gain. Two conditions might occur in dividers, the numerator signal is larger than the denominator's and vice versa. The gain of our proposed circuit can be adjusted independently in both conditions via a control signal and hence, offers the maximum level of gain adjustability.

II. PROPOSED CIRCUIT

Suppose x and y are analog signals (current or voltage) and our goal is to produce a signal that is proportional to the division of x and y as follows:

$$z = k \frac{x}{y} \quad (1)$$

where x in the numerator, y is the denominator, k is the gain of division and z is the final output. The straightforward solution to realize a divider is to use the analog dividers. However, as it was mentioned earlier, analog dividers have some limitations. Another solution is the use of digital signal processor, nevertheless, this method requires two ADCs to convert input signals to digital and a DAC to produce the analog signal from the division result. Our proposed circuit needs only an ADC and a DAC with similar resolution as depicted in Figure 1.

The ADC sampled and converts the input signal (x_{num}) based on its reference signal level (x_{den}) and its resolution (N bits) as follows:

$$x_{num} = \frac{x_{den}}{2^N} B \quad (2)$$

where B is an N -bit digital code. Applying the digital code to a DAC with similar resolution results to producing an analog signal as represented in (3).

$$x_{out} = \frac{x_{ref}}{2^N} B \quad (3)$$

Solving (2) and (3) we come to (4):

$$x_{out} = x_{ref} \frac{x_{num}}{x_{den}} \quad (4)$$

with the quantization error of $\pm x_{den} / 2^{N+1}$. Two situations might occur: numerator is bigger than the denominator and vice versa. They can be considered separately.

A. Denominator is Bigger Than the Numerator ($y > x$)

In this situation, the output signal resulting from (1) is less than k. Figure 2 shows the proposed circuit configuration to produce the output signal in this mode. Denominator signal (y) is connected to the reference signal pin of ADC (x_{den}) and Numerator (x) is connected to the input of the ADC (x_{num}). ADC voltage source (k_1) is connected to the reference signal of the DAC, and the final output is appeared on the output of the DAC based on (5).

$$z = k_1 \times \frac{x}{y} \quad (5)$$

Since in this mode, $x < y$, then for fixed k_1 , the produced output is the scaled version of the desired result. The amplification coefficient can be chosen arbitrarily based on the dynamic range of the DAC. Therefore, no extra amplification stage is required, and the output dynamic range of the output signal is in the range of $[0, k_1]$.

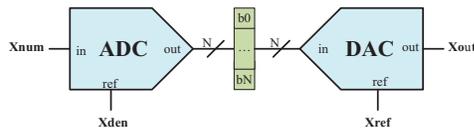


Fig. 1. The general configuration of our proposed circuit.

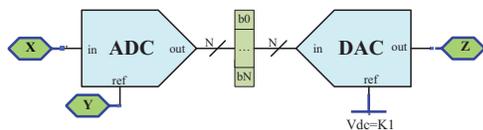


Fig. 2. The configuration of the circuit when $x < y$.

B. Numerator is Bigger Than the Denominator ($x > y$)

In this situation, the division result is greater than k. The connectivity diagram of the circuit in this mode is illustrated in Figure 3. In this situation, x is used as reference voltage of ADC (x_{den}) and y is connected to the input of ADC (x_{num}). Equation (6) shows the final output produced by DAC.

$$x_{out} = x_{ref} \frac{y}{x} \quad (6)$$

Since $x > y$ so the output swings from zero to x_{ref} like the first mode. The output signal generated in this mode is the inverse of the desired signal. Finding x_{ref} from above equation we have:

$$x_{ref} = x_{out} \times \frac{x}{y} \quad (7)$$

DAC produces an analog signal based on its resolution, reference signal and the applied digital code. The digital code is already produced by ADC and is constant between cycles. Suppose we compare the x_{out} signal with a constant signal (e.g. k_2). Rising x_{ref} gradually from zero, increases the output signal (x_{out}) as well. At the time that the output signal reaches k_2 , the x_{ref} signal has a value proportional to the division result as proved in (8).

$$x_{ref} = k_2 \times \frac{x}{y} \quad (8)$$

So the x_{ref} is the scaled version of desired output (z). ADCs have internal sample and hold that capture the input signal at the specific time produced by a clock generator. Then the conversion process is performed on the sampled signal. Our proposed circuit is suitable to be used in the sampled analog system in which the output signal is valid in specific time and between time slices, the signal processing is done in internal circuits. Therefore, between time steps, the digital code produced by ADC would not change. A ramp generator is used to produce the reference signal for DAC. It's simply a sawtooth signal generator with reset capability. Since the digital code is not changing, increasing the x_{ref} signal results in increasing the output of the DAC as well. The output signal produced by DAC is compared by a constant value (i.e. k_2) by a comparator. When the output signal is low, the comparator output is at the low saturation level, too, and the switch is opened. Increasing the x_{ref} , increases the x_{out} and this process is performed until the positive and negative voltages of comparator become equal. At this time, the comparator output signal flips to high saturation level. Consequently, the switch turns on and x_{ref} connected to the output pin (z). Meanwhile, the ramp generator is being reset in order to start the new cycle, resulting in decreasing x_{out} and turning off the switch. Figure 4 depicts the internal structure of the ramp generator. The sawtooth signal is generated by a PMOS current source (MP1) and an integrating capacitor (C). NMOS switch is connected in parallel to the capacitor in order to discharge it during reset phase. Since x_{clk} and enable signals are not allowed to be activated simultaneously, direct current path from Vdd to gnd cannot be created, which means no extra static power is dissipated. It is worth mentioning that ramp generator is solely used in second mode where the numerator is bigger than the denominator. Using enable signal makes it possible to deactivate the circuit in the first mode.

C. Complete Circuit

Combining the abovementioned circuits, the final structure of the proposed circuit can be achieved as shown in Figure 5.

This circuit has two signal paths that activate based on the modes describe before. This is done by comparing the numerator and denominator signals. Analog multiplexers are used to form the signal path. In Figure 5, the input signals are compared by the comparator (Comp2) which generates the sel signal. Suppose x is greater than y then sel would be at low saturation level results in selecting the zero line of the multiplexers. Therefore, y signal is applied to the input and x is applied to the reference of ADC. This is the second mode which utilizes the ramp generator. Hence the ramp generator is enabled by the sel signal (turning on MP2), and the sawtooth signal (x_{ramp}) is applied to the reference of the DAC (x_{ref}). In this configuration, the x_{ref} signal is applied to the output pin through Mux4 ($z=x_{ref}$). As it is mentioned earlier, this signal is equal to the division result scaled by k_2 . If $x < y$, then sel signal is high and x is applied to the input of the ADC and y to its reference pin. The ramp generator disabled (MP2 is off), and the x_{ref} is connected to k_1 voltage source. In this mode, the output signal generated by DAC is connected to output pin (z). Data converters are reported in the literature both in current and voltage mode [16-21]. They are designed in a wide variety of methodologies such as: Flash, successive approximation, pipeline and sigma delta. The selection of the data converter is based on the nature of input and output signals. While the ADC type is determined by the input signal nature, output signal is a criterion for DAC selection. Since both current and voltage mode data converters work with digital code, using different architectures makes it possible for the designer to manage a trade-off between speed, cost and power consumption based on the desired input and output signal nature. In Table I, the different selection guideline is summarized.

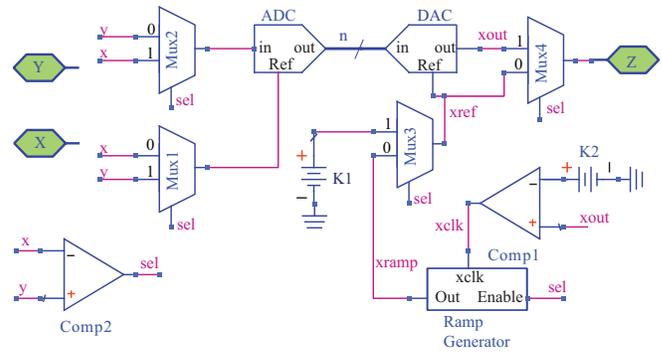


Fig. 5. The complete structure of the proposed circuit.

TABLE I. DATA CONVERTER SELECTION GUIDE

Input signal	Output signal	ADC type	DAC type
voltage	voltage	Voltage mode	Voltage mode
voltage	current	Voltage mode	current mode
current	voltage	current mode	Voltage mode
current	current	current mode	current mode

III. SIMULATION RESULTS

The proposed circuit is simulated in HSpice. The generic model of ADC and DAC with 8-bit resolution is used in the simulation environment. The transient simulation is done in three different conditions.

A. State 1 ($x < y$)

In this situation, the signals defined in Table II are applied in the simulation engine as depicted in Figure 6. Simulation is performed for two different k_1 values. In Figure 7a the results when k_1 is considered to be 1V is depicted. The green curve shows the ideal output while the red one is the result produced by the circuit. The sampling frequency is considered to be 100Khz. Figure 7b shows the output signal when $k_1=2V$. As it can be seen, the output is doubled when increasing k_1 from 1V to 2V.

B. State 2 ($x > y$)

In this state, the numerator is fixed at 120mV using a DC source, while a 1kHz sine wave with 20mV AC amplitude and 0.1V of DC offset is applied to the denominator input pin as depicted in Figure 8a. Figure 8b shows the ideal as well as the actual output signal when the sampling frequency is 10kHz. The output signal generated by DAC (x_{out}) and the comparator output (x_{clk}) are illustrated in Figure 8c. When the x_{ref} is rising from zero, x_{out} increases as well. This process continues until x_{out} is becoming equal to k_2 , where the x_{out} has a value equal to the division result. Simultaneously, the comparator output flips to high saturation level disabling the ramp generator. Halving the k_2 signal to 0.5V, halving the final output as well as illustrated in Figure 8d.

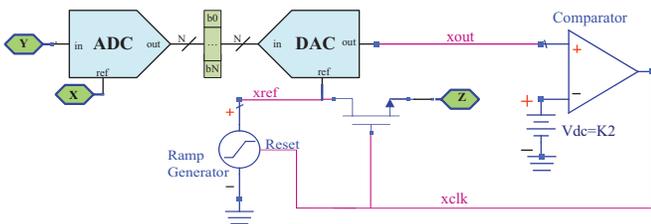


Fig. 3. Circuit diagram in the second mode ($x > y$).

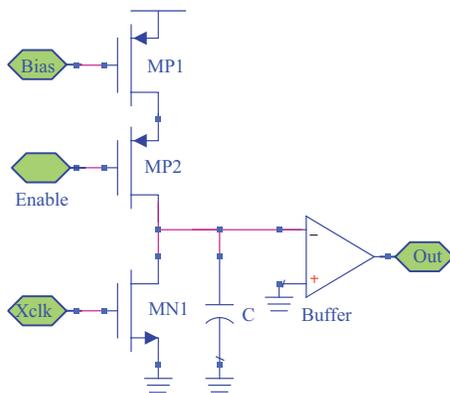


Fig. 4. Internal structure of the ramp generator.

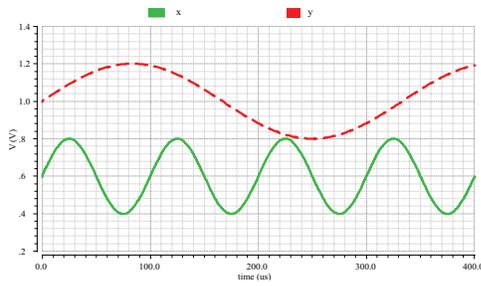


Fig. 6. Numerator (green) and denominator (red) signals applied to the circuit in 1st state ($x < y$)

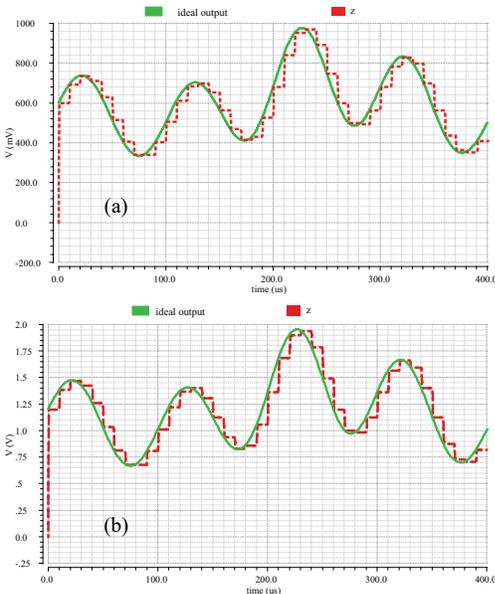


Fig. 7. Simulation results in the first state ($x < y$). ideal (green) and actual (red) result produced when (a) $k_1=1V$ and (b) when $k_1=2V$.

C. State 3

In the final simulation run, the overall performance of the system is examined using arbitrary input signals as characterized in Table III and plotted in Figure 9a. In this situation, both modes are used because sometimes the numerator is bigger than the denominator, and the opposite in other times. Figure 9b shows the simulation results with 10Khz of sampling frequency. As it is shown when x is greater than y , x_{out} is rising from zero and converges to the output result equal to the sampling time otherwise the output signal is generated by the circuit configuration described in the first mode.

TABLE II. SIGNALS USED IN STATE-1 SIMULATION

Signal name	Signal attribute		
	Frequency (kHz)	Amplitude (mV)	DC offset (V)
Numerator (x)	10	200	0.6
Denominator (y)	3	200	1

TABLE III. SIGNALS USED IN STATE-3 SIMULATION

Signal name	Signal attribute		
	Frequency (kHz)	Amplitude (mV)	DC offset (V)
Numerator (x)	3	50	0.12
Denominator (y)	1	20	0.1

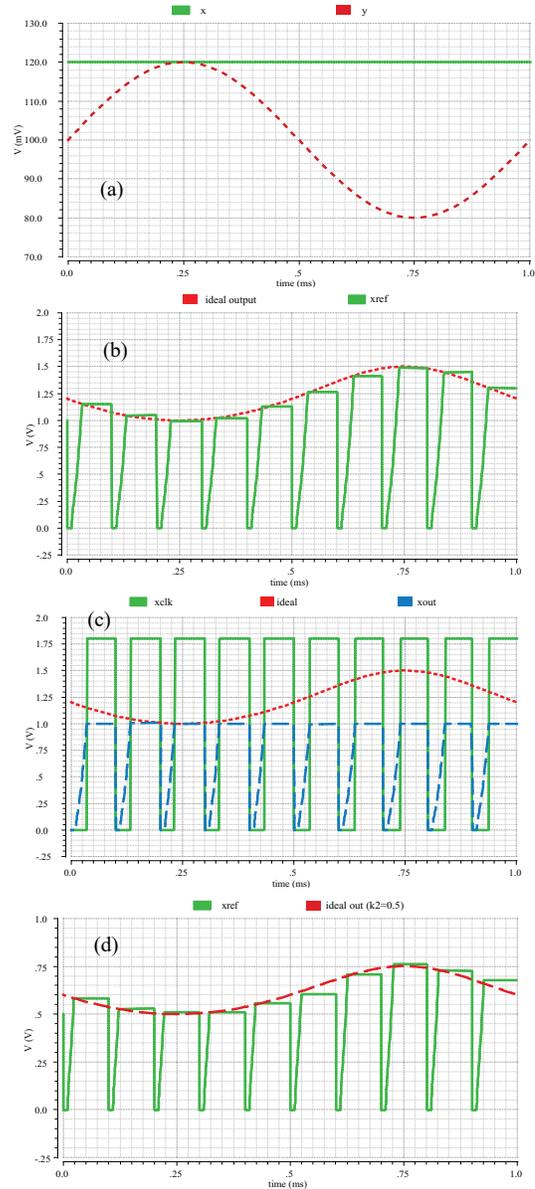


Fig. 8. Simulation results in 2nd state ($x < y$). (a) Numerator (green) and denominator (red) signal in 2nd state (b) ideal (green) and actual (red) result output signal when $k_2=1V$ (c) DAC (blue) and comparator (green) output signal generated when $k_2=1V$ ideal output (red) signal is also plotted (d) output signal (green) and ideal output (red) when $k_2=0.5V$

IV. CONCLUSION

In this paper, a novel divider/defuzzifier circuit is presented. Using data converters makes it possible to design a divider with wide dynamic range. The speed, power consumption and dynamic range are limited by the data

converter specification used. By proper component selection, a designer can manage the trade-off between above-mentioned parameters. The gain of the circuit is controlled by two different DC sources, each of them utilized in specific situation, i.e. when the numerator signal is bigger than the denominator and vice versa. Another advantage of our proposed method is that one can use different data converters based on the nature of desired input and output signal. For example, having a voltage mode ADC and current mode DAC, means the input signals are voltage while the output is a current signal.

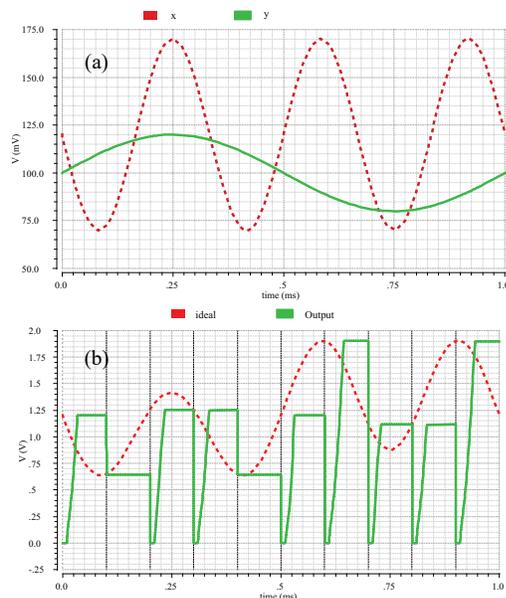


Fig. 9. Simulation results in the 3rd state. (a) Numerator (red) and denominator (green) signal (b) ideal (red) and actual (green) result output signal when $k_1=k_2=1V$.

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