An Optimized Multilevel Inverter Topology with Symmetrical and Asymmetrical DC Sources for Sustainable Energy Applications

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Abstract—**This paper proposes an optimized Multi-Level Inverter (MLI) topology with symmetrical and asymmetrical DC sources for sustainable energy applications. The proposed MLI has optimized components to reduce size, cost, and installation area in comparison with traditional MLIs. It also improves output power quality by reducing harmonics in the stepped output, and hence it can be used for sustainable energy applications with a grid interface. The proposed inverter is equipped with six switching devices, one clamping diode, and two DC sources. It produces a five-level stepped output when using symmetrical DC sources and a seven-level stepped output when using asymmetrical DC sources. In this topology, the six switching devices are divided into two units, namely the level generator and the polarity generator units, the switches used in the level generator are responsible for producing the required number of levels in the form of rectified stepped output and the switches used in the polarity generator are responsible for converting the rectified stepped waveform to stepped AC output. The simulation results verify the operation of the MLI when fed with linear load with symmetrical and asymmetrical DC sources, and the experimental output results are presented for validation.**

Keywords-optimal multilevel inverter; symmetrical; asymmetrical; total harmonic distortion

I. INTRODUCTION

Multi-Level Inverters (MLIs) are popularly used devices for power conversion in grid-connected systems, industrial applications, electric vehicles, Uninterruptible Power Supply (UPS) devices, FACTS devices, etc. MLIs are capable of generating an output voltage with near sinusoidal wave shape. In addition, they have features like producing output with reduced Total Harmonic Distortion (THD), reduction in power losses due to the lower switching frequency, reduced dv/dt stress and un-necessity of filters which results in size and cost reduction of the overall inverter [1-4].

The classical topologies of MLIs are diode clamped MLI or Neutral Point clamped (NP-MLI) [5], Flying Capacitor MLI (FC-MLI) [6] and Cascaded H-bridge MLI (CH-MLI) [7], and are used in various industrial applications. However, NP-MLI and FC-MLI suffer from limitations compared to CH-MLI, limitations such as the larger number of switching devices, the requirement of clamping diodes and capacitors, voltage-unbalancing issues across the capacitors etc. Due to the simple structure of CH-MLI, it can be easily integrated with renewable energy sources. Over the last years, research has focused on emerging topologies to overcome the limitations of the conventional MLI. CH-MLI consists of H-bridges with independent DC sources across each bridge. The magnitude of all voltage sources can be either the same or different. In symmetric CH-MLI, the magnitude of all voltages sources will be equal, whereas in asymmetric CH-MLI, the magnitude of all voltage will be different [8, 9]. The asymmetric inverters generate more levels in output as compared with symmetric MLIs with the same topology or the same number of power electronic switches and sources. Therefore, cost, size, complexity, THD, and losses of the asymmetric inverters are reduced [12]. Authors in [13-15] tried to reduce the number of switches to overcome the cost constraint, and improve the quality of output voltage waveform by increasing the number of levels in the output voltage.

This paper presents a single-phase MLI topology with symmetrical and asymmetrical voltages, which uses a reduced number of components compared to the existing topologies

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[16-18]. This configuration is the extension of the topology proposed in [10], which can be extended to three-phase [17].

II. PROPOSED TOPOLOGY

Similar to the recently introduced hybrid MLIs, the proposed inverter also consists of two circuits. The first one is a level generating circuit, it works at the fundamental or at a high frequency and the second one is the H-bridge circuit operating at the fundamental frequency. The first circuit generates a positive stepped waveform across the H-bridge and the second generates positive and negative stepped waveforms in the output voltage. The generalized figure of the proposed optimized MLI is presented in Figure 1. The circuit can be powered with symmetrical or asymmetrical voltage. In the symmetrical topology, all input voltage magnitudes are maintained at equal values: V_1: V_2:V_3:V_4 : : : V_k=1:1:1:1 : : : 1 and in the asymmetrical voltage topology, the voltages are maintained with the ratio of V_1:V_2: V_3:V_4: : : : V_k = 1 : 2 : 3 : 4 : : : k, where: k represents the number of voltage sources. The level generating circuit is used for generating the positive stepped voltage levels across the H-bridge. It consists of voltage sources, level generating switches, and diodes to prevent the reverse of the current. The H-bridge circuit is used for polarity reversal, it is responsible of producing the positive and negative stepped voltage levels at the output and it consists of four switches.

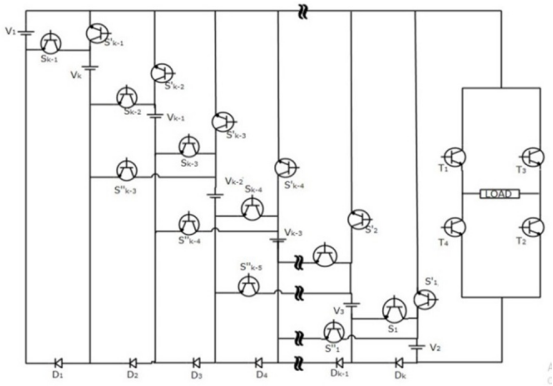

Fig. 1. Generalized structure of the proposed optimized MLI

The required number of output levels, control switches, and diodes with n_s sources for the optimized MLI with symmetrical voltages are:

- Levels generated in output with n_s sources = $(2n_s + 1)$
- Control switches required to generate n levels with n_s sources = $(3n_s -1)$, for n ≥3
- Diodes required for generating n levels = $(n_s - 1)$
- Peak output voltage = $(2n_s+1)\times V_{dc}$

The output levels, control switches, and diodes for the optimized MLI with unsymmetrical voltages are:

- Levels generated in output with n_s sources = $n_s (n_s + 1) + 1$
- Control switches required to generate n levels with n_s sources = $(3n_s -1)$, for n ≥3
- Diodes required for generating n levels = $(n_s - 1)$
- Peak output voltage = $(n_s\times(n_s + 1) +1)\times V_{dc}$

III. SYMMETRICAL AND ASYMMETRICAL OPTIMIZED MLI

To explain the operation of the MLI shown in Figure 1, two voltage sources with equal or unequal magnitude are considered (Figure 2).

A. Operation of Symmetrical Optimized MLI

With two symmetrical sources (V_1:V_2 = 1:1), the proposed MLI shown in Figure 2 is capable of generating 5 levels at the output terminals, utilizing 2 DC sources, 6 control switches, and 1 diode. When compared with the conventional and recently proposed MLIs, this topology requires a reduced number of power electronic switches, hence it is characterized by reduced size, controllability and switching losses. Among the six switches, T_1, T_2, T_3, and T_4 are H-bridge switches, also called polarity reversing switches and the switches S_1 and S_1^1 are level generating switches. The various switching states for generating 5 levels at the output are shown in its switching table (Table I). The first positive stepped (V_{dc1}=V_1) level is achieved by turning on the H-bridge switches T_1 and T_2 and the diode or level generating switch S_1^1. The second level (V_{dc2} = V_1+V_2) is obtained by turning on the H-bridge switches T_1 and T_2 and the level generating switch S_1. During this instant, the diode D will not conduct, as a negative voltage is applied to the diode.

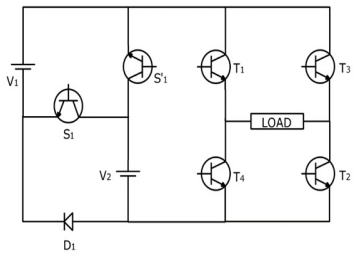

Fig. 2. The optimized MLI with two symmetrical or asymmetrical voltage sources

TABLE I. SWITCHING SEQUENCE TO GENERATE FIVE LEVELS WITH TWO SYMMETRICAL SOURCES

Output voltage	H-bridge switches				Level generating switches	
	T_1	T_2	T_3	T_4	S_1	S_1'
V_1+V_2	1	1	0	0	1	0
V_1	1	1	0	0	0	0
	1	1	0	0	0	1
0	1/0	0/1	1/0	0/1	0	0
$-V_1$	0	0	1	1	0	0
	0	0	1	1	0	1
$-(V_1+V_2)$	0	0	1	1	1	0

The zero switching states can be obtained in two ways: one is using the H-bridge switches T_1, T_3, and the load and the other is using the H-bridge switches T_2, T_4, and the load. Similarly, the negative stepped voltages are achieved by turning on the H-bridge switches T_3 and T_4 instead of T_1 and T_2 as in the case of positive voltage levels. All the gates are signaled by a simple Pulse Width Modulation (PWM) technique, in which a sinusoidal reference signal is compared

with the carrier signal for generating the gate signal. These signals or pulses are ANDed and ORed by a logical operator to obtain the required pulses. These final pulses are then given to the corresponding switches.

B. Operation of the Asymmetrical Optimized MLI

The 5-level topology shown in Figure 2 is capable of generating 7 levels at the output terminals with two asymmetrical voltage sources. The two DC sources are considered with the ratio of 1:2. The various switching states for generating a 7-level output are given in Table II. The lower level positive stepped waveform is obtained by turning on the H-bridge switches T_1 and T_2 and the diode, the positive middle level can be obtained by turning on the level generating switch S_1^1 along with H-bridge switches T_1 and T_2, and the highest level at the output is obtained by turning on the H-bridge switches T_1, T_2 and the level generating switch S_1. Similarly, the negative stepped voltages are achieved by turning on the H-bridge switches T_3 and T_4 instead of T_1 and T_2.

TABLE II. SWITCHING SEQUENCE TO GENERATE SEVEN LEVELS WITH TWO UNSYMMETRICAL SOURCES

Output voltage	H-bridge switches				Level generating switches	
	T_1	T_2	T_3	T_4	S_1	S_1'
V_1+V_2	1	1	0	0	1	0
V_2	1	1	0	0	0	1
V_1	1	1	0	0	0	0
0	1 /0	0/1	1/0	0/1	0	0
$-V_1$	0	0	1	1	0	0
$-V_2$	0	0	1	1	0	1
$-(V_1+V_2)$	0	0	1	1	1	0

IV. COMPARISON WITH EXISTING TOPOLOGIES

To show the advantages and the originality of the proposed optimized MLI, the data of conventional, recent, the proposed topologies are presented and compared in this section. The control difficulty and consistency directly depends on the number of required power electronic switches. The detailed comparison data are listed in Table III.

TABLE III. SYMMETRICAL MLI COMPARISON

	[2]	[3]	[4]	[10]	[11]	Proposed
Main switches	2(n-1)	2(n-1)	2(n-1)	2(n-1)-2	$\frac{(n+7)}{2}$	$\frac{(3n-5)}{2}$
Clamping diode	(n-1)(n-2)	0	0	(n-3)(n-2)	0	$\frac{(n-3)}{2}$
Flying capacitors	0	$\frac{(n-1)(n-2)}{2}$	0	$\frac{(n+1)}{2}$	$\frac{(n-1)}{2}$	0
DC bus capacitors	(n-1)	(n-1)	0	$\frac{(n-1)}{2}$	$\frac{(n-3)}{2}$	0
DC source	1	1	$\frac{(n-1)}{2}$	1	1	$\frac{(n-1)}{2}$
Total components	n^2	$\frac{(n^2+3n-2)}{2}$	$\frac{(5n-5)}{2}$	n^2-2n+3	$\frac{(3n+5)}{2}$	$\frac{(5n-9)}{2}$

Figure 3 represents the total devices required for generating the specific level. The proposed structure requires a comparatively very small number of switches with symmetrical or with asymmetrical voltage, and at any instant a maximum of 4 switches will conduct.

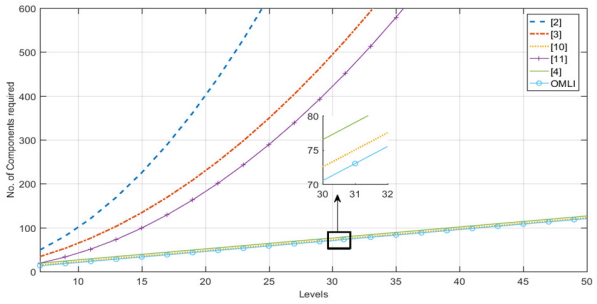

Fig. 3. Total number of required components

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

In order to verify the performance of a proposed MLI, it was simulated in MATLAB/Simulink platform with a linear load. The simulation results of the proposed MLI with two symmetrical sources (V_1:V_2=100:100) and two asymmetrical sources (V_1:V_2 = 100:200) are discussed in this section. Figure 4 shows the Simulink model of the Optimized MLI (OMLI).

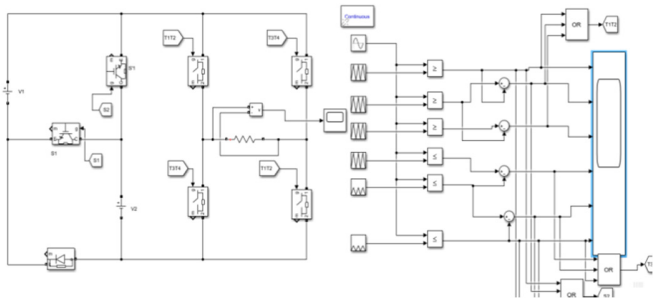

Fig. 4. Simulink model of the proposed PLI

The output voltage, output current, and THD present in the voltage of the 5-level proposed OMLI with two symmetrical DC sources are shown in Figure 5.

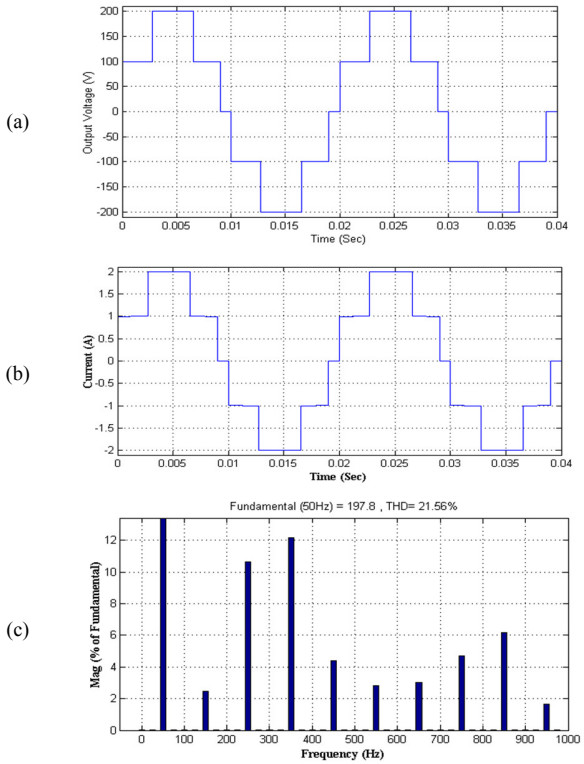

Fig. 5. (a) 5-level voltage, (b) 5-level current, (d) FFT analysis with two symmetrical sources

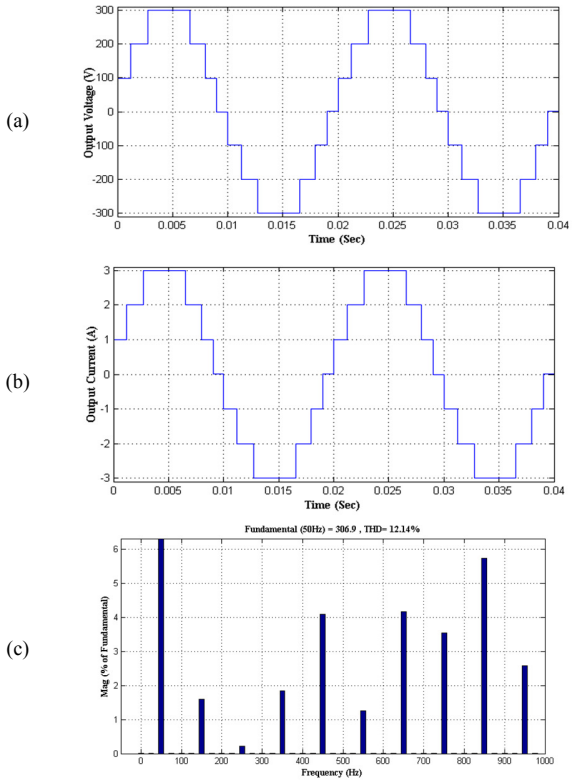

Fig. 6. (a) 7-level voltage, (b) 7-level current, (c) FFT analysis with two asymmetrical sources

To run the OMLI Simulink model, Ode 45 solver has been used with a run time of 0.04s for two cycles. Form Figure 5(a) and 5(b) it is observed that each level has a step change of 100V and 1A respectively. The %THD value of OMLI for the 5-level is 21.56% as shown in Figure 5(c). Output voltage, output current, and THD present in the voltage of the 7-level OMLI with two asymmetrical DC sources are shown in Figure 6. Form Figure 6(a)-(b) it is observed that each level has a step change of 100V and 1A respectively. The %THD in output voltage is 12.14, having reduced by 44% when compared to the 21.56%.

B. Experimental Results

The proposed OMLI with two asymmetrical DC sources was tested experimentally in order to evaluate its performance. The prototype of the OMLI is shown in Figure 7 and the experimental results in Figure 8.

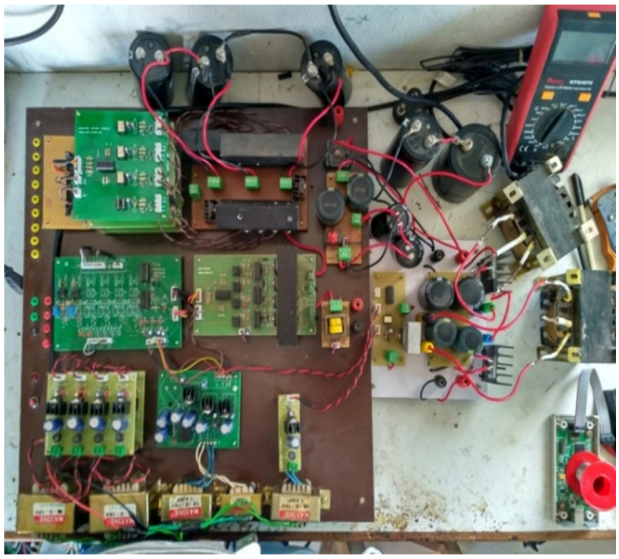

Fig. 7. Photograph of hardware setup of the proposed MLI

The implementation of the proposed MLI was carried-out by using an FPGA Spartan-6 controller, which is highly preferable to generate switching pulses in real-time implementations with an Xilinx processor as IR2110 driver module and TLP250 Opto-Couplers. The power semiconducting switches used in the experimental prototype model are 6 Nos of FGA15N120 IGBTs with anti-parallel diodes and one uncontrolled switch. The outcome waveforms were measured and recorded with key-sight DSOX2014A Oscilloscope, with a 100MHz, 4 Analog Channels. From the simulation analysis, it was observed that the OMLI output voltage THD for the 7-level inverter was 12.14%. The THD of the prototype model was measured with a FLUKE 434 series-II power-quality analyzer and the results are presented in Figure 8(a) and (b). Figure 8(a) shows the 7-level output voltage of the OMLI with asymmetrical sources and Figure 8(b) shows the corresponding %THD which was 13.1% for the 7-level OMLI. From Figure 8, it is clear that the experimental results are in close agreement with simulation and theoretic analysis with an acceptable error of ±2%.

(a)

(b)

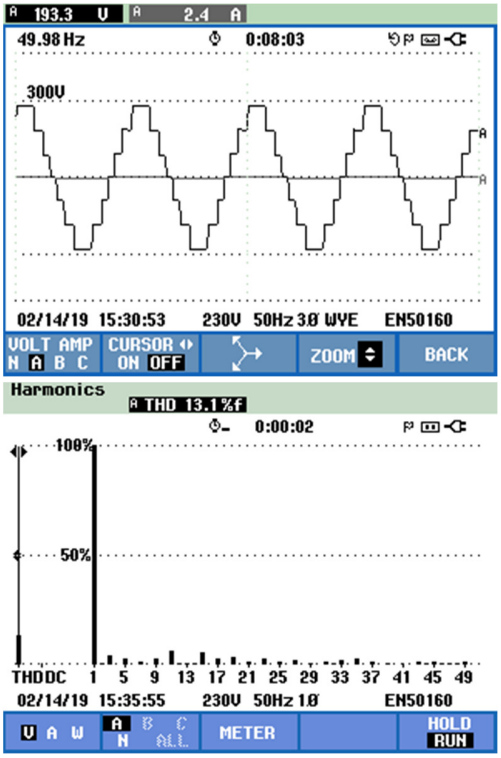

Fig. 8. (a) 7-Level voltage (b) corresponding THD

VI. CONCLUSIONS

In this work, an optimized multilevel inverter has been presented for sustainable energy applications. In comparison with the already existing and recently proposed topologies, this topology uses fewer components to produce the steps at the output side. Thereby, the proposed inverter will be compact in size and its overall complexity will be reduced. The proposed inverter was simulated in MATLAB/Simulink with the consideration of two symmetrical or asymmetrical voltage sources. It was seen that, with two symmetrical sources, the proposed inverter produces 5 levels at the output side, while with two asymmetrical sources it produces 7 levels. The simulated performance of the proposed 7-level inverter has been compared with the experimental results, which are in close agreement with the simulation results.

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