Design of a Low Power CMOS Inverter with the V_{BB} Stack Approach

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Abstract-Due to the exponential advancement in nanotechnology devices, low energy consumption has become a significant concern of researchers and VLSI designers. In this paper, the Variable body bias (V_{BB}) and the stack approach are used simultaneously to reduce the leakage power of a CMOS inverter in standby mode. This new technique is called the V_{BB} stack approach. The simulations have been conducted on the LT spice simulator. The power evaluation has been determined and compared between the conventional approach, the stack approach, and the V_{BB} stack approach. The results have demonstrated the performance of the V_{BB} stack approach. The power consumption in the V_{BB} stack approach has decreased by 23% compared to the conventional approach and by 10% compared to the stack approach.

Keywords-CMOS inverter; VLSI; power dissipation; leakage current; low power; V_{BB} stack approach

I. INTRODUCTION

The continuous demand for lightweight portable devices such as laptops, tablets, and smart phones has increased the need to reduce the processor size [1, 2]. VLSI designers have made possible to put millions of transistors on a single chip while maintaining good device performance [3]. The oxide thickness of transistor has been shrinking. The channel length has also become short, but produces increased leakage current in standby mode. With the continuous decreasing of technology size, the leakage power in standby mode is becoming the main contributor of total power consumption. The high power dissipation has become a major issue in digital circuit design with each new technology emergence [4]. The main effect of high leakage power is the increase in temperature, which in some cases leads to device breakdown [5]. Power optimization has become an important research field for VLSI designers. Many techniques have been proposed, each one delivering a new way to decrease power leakage, but the shortcomings of each push researchers to try to discover a better approach. In this work, the stack approach and the V_{BB} approach are used simultaneously to ensure the best power optimization of a CMOS inverter. The proposed technique is called the V_{BB} stack approach.

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II. LITERATURE REVIEW

At all levels of VLSI design steps, many approaches heve been proposed to reduce power dissipation. Authors in [6] presented low power half adder, full adder, half substractor, and full substractor using the CMOS technology. Authors in [7] developed a full adder design using the modified GDI technique to reduce power consumption. Authors in [8] analyzed a MOS transistor to decrease leakage current in standby mode based on forward and reverse body biasing techniques. Authors in [9] used the substrate biasing technique to reduce the standby leakage power of a nanometer scale CMOS circuit. The substrate biasing V_{SB} of a CMOS transistor has a direct effect on the threshold voltage V_{th}, which can be controlled by varying the substrate potential. The equation that shows the impact of substrate biasing on threshold voltage is:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\emptyset_B - V_{SB}|} - \sqrt{|2\emptyset_B|}) \quad (1)$$

where $\emptyset_B$ is the flatband voltage, γ is the substrate effect coefficient, V_{th0} is the threshold voltage with zero body biasing, and V_{SB} is the source to substrate voltage.

The threshold voltage is directly proportional with the body potential V_{BB} (V_{SB}). Figure 1 illustrates the conventional CMOS connections and the V_{BB} connections.

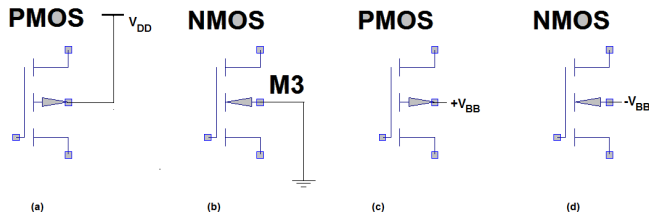

Fig. 1. Body connections: (a), (b) conventional bias, (c), (d) V_{BB} technique.

Commonly, the body (substrate) of an NMOS transistor is connected to the ground and the body of the PMOS transistor is connected to V_{DD} [10]. With the V_{BB} technique, the body terminal of PMOS is connected to the positive voltage, and the body terminal of NMOS is connected to the negative voltage to increase the threshold voltage. Authors in [11] presented the stack technique as a method to reduce leakage power. This method is based on the principle that each transistor can be replaced by two half size transistors associated in series [11, 12].

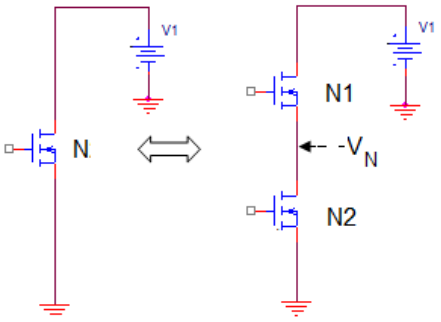

Fig. 2. The stacking technique.

If only one transistor "N" is in standby mode, the potential in the source node is zero, hence there is not a self-reverse bias effect and the leakage current increases. When both transistors N1 and N2 are in standby mode, a low drain current occurs. A positive potential V_N appears. The gate to source voltage (V_{GS1}) of transistor N1 reduces because the sub-threshold current reduces which has as effect an increase to the threshold voltage. This effect is known as the stacking effect [13]. Authors in [11] used the sleepy stack approach to reduce the power consumption of a CMOS inverter. The sleepy stack approach consists of dividing each transistor into two half size transistors. A sleep transistor is placed in parallel to one of the transistors. During the standby mode, the sleep transistors are put off. The threshold voltage increases and the leakage current reduces. The increase of area is the major penalty of this approach. Authors in [14] used the MTCMOS technology to design of a low power XNOR gate. This method is based on adding two sleep high threshold voltage transistors to the principal circuit. While low threshold transistors are active to realize the principal function, the high threshold transistors are turned on. During the stand-by mode, the high threshold transistors are turned off, hence the subthreshold leakage current is cut off and the static power decreases. The MTCMOS technique reduces the leakage current but increases the propagation delay time.

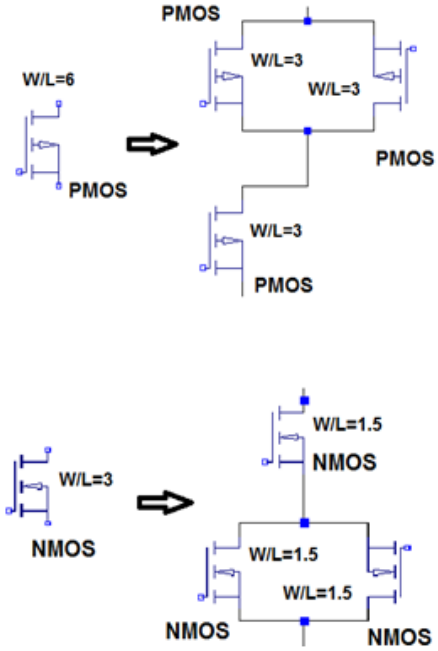

Fig. 3. The sleepy stack approach.

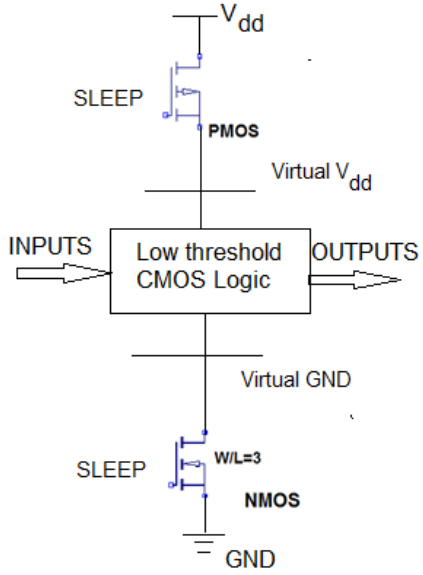

Fig. 4. The MTCMOS technique.

Authors in [15] proposed the use of the LECTOR technique to cut down the leakage current of a NAND gate [17]. In this approach, two leakage control transistors LC1 and LC2 are introduced between the pull up and pull down network. The source of each leakage transistor controls the gate terminal of the other. The introduction of leakage control transistors increases the resistance between V_{dd} and Gnd, thus reducing the leakage current. The lector technique reduces the leakage current but increases the area and the propagation delay time.

III. LOW POWER INVERTER USING THE V_{BB} STACK APPROACH

The inverter is the basic design element of digital circuits. A good understanding of its behavior is necessary in order to build more complex circuits. It has one input and one output.

The output is always the complement of the input. Which means a logical 0 at the input produces a logical 1 at the output and vice versa [10, 11]. Generally, a CMOS logic circuit consists of a symmetrical and complementary pairs of PMOS blocks placed on the circuit as a pull up Network (PUN) and a NMOS block connected as a PULL- down network (PDN). The conventional CMOS inverter consists of two complementary transistors connected to the same input.

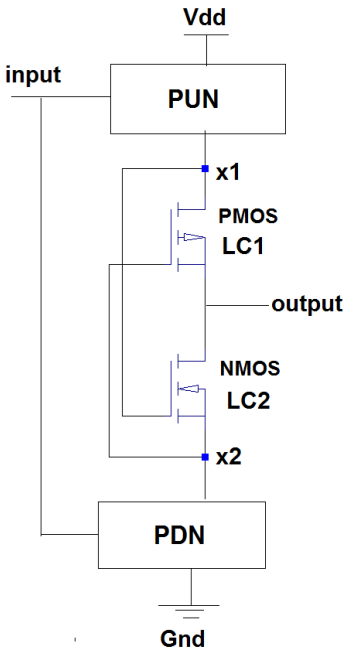

Fig. 5. The LECTOR technique.

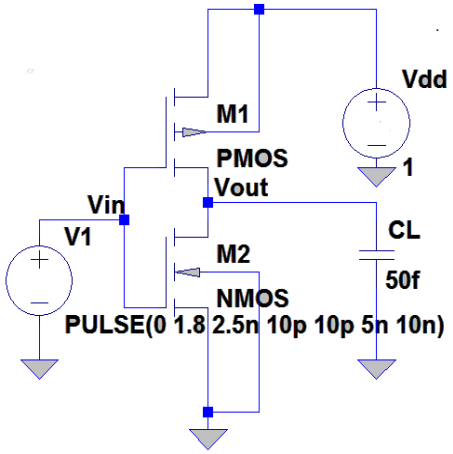

Fig. 6. The conventional CMOS inverter.

In active mode, the transistors behavior is comparable to that of switches. When the input is at low logic level (0), the P-MOS transistor is conductive and acts like a closed switch, the Current flows from the V_{dd} supply to the output. When the inverter input is at high logic level (1), the PMOS transistor is cut off, disconnecting the output from the positive voltage V_{dd} and the N-MOS transistor is conductive and acts like a closed switch, pulling the output to low level (0). The power dissipation in the CMOS inverter consists of two components, the dynamic and the static power. Dynamic power permits to charge and discharge the load during the active mode [12]:

$$P_{dyn} = C_L * V_{dd}^2 * f \quad (2)$$

where C_L is the load capacitance, V_{dd} is the supply voltage. Ideally a PMOS transistor must be in standby mode when $V_{es} < V_{th}$ (static power), V_{es} is the voltage from the gate to the source, and V_{th} is the threshold voltage.

Due to reduced transistor size, the gate oxide and the channel length become short which produces leakage power or static power. As reported by VLSI designers, static power may in the future dominate the total power consumed by CMOS devices as technology size continue to shrink [10, 16]

$$P_{static} = V_{dd} * I_{leakage} \quad (3)$$

where $I_{leakage}$ is the leakage current during the standby mode.

A major part of the leakage current is caused by the sub-threshold current [12].

$$I_{sub} = I_{sub0} e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \quad (4)$$

where I_{sub0} is the zero bias electron mobility:

$$I_{sub0} = \mu_{eff}.C_{ox}\left(\frac{W}{L}\right).V_T^2 \quad (5)$$

where V_T is the thermal voltage, V_{th} is the threshold voltage, η is the sub- threshold swing coefficient, V_{gs} is the transistor gate to source voltage, V_{ds} is the drain to source voltage, μ_{eff} is the electrons mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the width and length of the channel respectively.

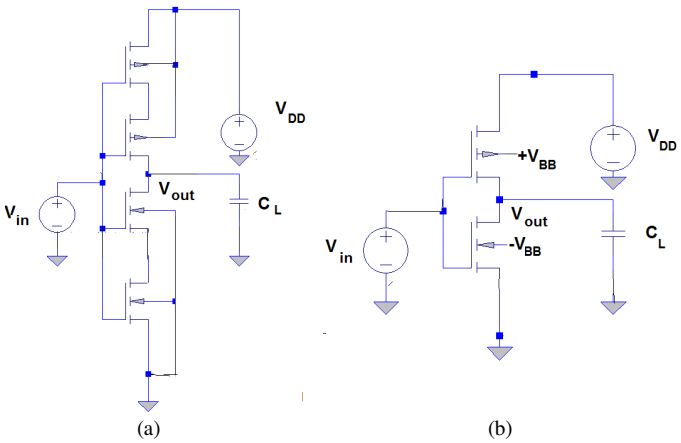

Fig. 7. Low power CMOS inverter (a) stack method, (b) V_{BB} method.

The sub- threshold current I_{sub} is inversely proportional to the threshold voltage V_{th}. Therefore, an improvement of the threshold voltage may resolve the problem of growing leakage power. The stack and V_{BB} techniques are frequently used to improve the threshold voltage in consequence decrease the leakage power in VLSI circuits and devices. Each method

increases the substrate potential in a different way which decreases the substrate leakage current. To take advantage of the stack and V_{BB} approaches, we have used them together in the same circuit. The new technique is called the V_{BB} stack approach. Each transistor in the conventional inverter is divided into two equal transistors. A positive potential is applied on the body terminal of PMOS transistors. A negative potential is applied on the body terminal of NMOS transistors. A self-reverse bias potential appears in all transistors, thus the threshold voltage increases and the leakage current decreases. The schematic circuit design and the simulation of the inverter with the V_{BB} stack approach have been done on the LT-Spice tool.

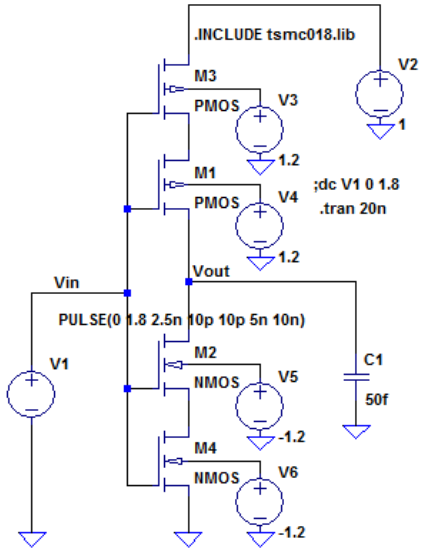

Fig. 8. Design of the inverter using the V_{BB} stack approach.

IV. RESULTS AND DISCUSSION

To evaluate the performance of the proposed method, the inverter is simulated on the LT-Spice with supply voltage variation from 0.2V to 1V. Simulations have been carried out for the inverter in the conventional approach, the stack approach, and the V_{BB} stack approach. Power dissipation and delay have been calculated with variation in V_{dd}.

TABLE I. POWER DISSIPATION AND DELAY VARIATIONS AS FUCTIONS OF THE SUPPLY VOLTAGE

Supply voltage (V)		0.2	0.4	0.6	0.8	1
Conventional approach	Power dissipation (nW)	111	615	1604	3044	4897
	Delay (nS)	7.757	7.757	7.510	7.493	7.441
Stack approach	Power dissipation (nW)	82	443	1214	2460	4197
	Delay (nS)	7.645	7.561	7.544	7.510	7.491
V_{BB} stack approach	Power dissipation (nW)	71	368	997	2036	3535
	Delay (nS)	7.634	7.562	7.561	7.527	7.508

From the obtained results, it is observed that power dissipation increases simultaneously when the supply voltage increases. Power dissipation in the V_{BB} stack approach is minimal in comparison with the other techniques, but the delay increases slightly due to the increase in the threshold voltage of the device. We can observe from Table I that by using the stack technique we can save 27% power as compared to the conventional method, but in this case the delay is increased slightly. By using the proposed V_{BB} stack technique, power dissipation is approximately 37% less than in the conventional method, but with a slight increase in delay of 2%. Figure 9 shows the power dissipation characteristics as functions of the supply voltage.

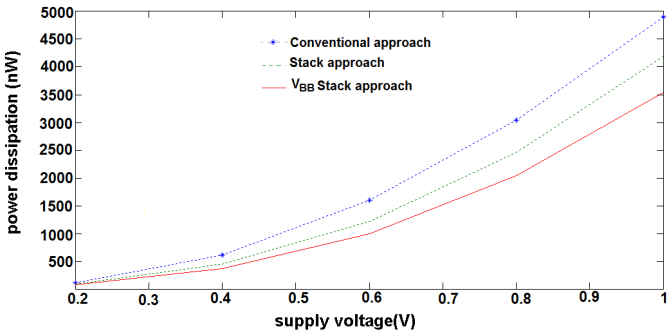

Fig. 9. Power dissipation characteristics.

The main achievement is the inverter with the proposed V_{BB} stack approach is that it shows much better performance in terms of consumed power as compared to the conventional and stack methods. Hence, the proposed V_{BB} stack approach technique is an optimum alternative method to realize low power devices with accepted performance in VLSI design.

V. CONCLUSION

The demand for low power VLSI circuits increases due to the continuous development of wireless technologies which require a limited source of power. Power dissipation is becoming a major issue in today's digital circuits. So, the main objective of VLSI designers is to reduce power consumption as much as possible. In this paper, the V_{BB} stack approach is presented as a solution to prevent the problem of leakage power. A comparative analysis of logic CMOS inverters that were designed with the conventional technique, the stack technique, and the V_{BB} stack technique was conducted in this paper. To evaluate the performance of the V_{BB} stack approach, all CMOS inverter designs have been simulated in LT-Spice, with supply voltage variation from 0.2V to 1V. From the experimental results, it is observed that power dissipation in the V_{BB} stack technique is much less than in the other techniques with a minor increase in delay.

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