A Novel Efficient Sine Wave Inverter with Custom Programmed PWM and Intelligent Control

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***Abstract*—This article presents an efficient design of a pure sine wave inverter which results in an electronic design with reduced losses. The proposed design incorporates the generation of custom programmed pulse width modulation (CPPWM) waveforms; the gate drive signals that are customized for the harmonic elimination from the output voltage, maximizing the fundamental component and resulting in an efficient electronic circuit design as compared to the traditional techniques in terms of the switching losses and the filtering energy losses. The CPPWM signals are digitally programmed in a micro-controller. The inverter realization is followed by an intelligent compensator design for the regulation of output voltage amplitude. The proposed algorithm self-adjusts its parameters in response to the load current and voltage amplitude variations hence resulting in an improved performance. The simulation results of the control algorithm are presented. The experimental validation of the theoretically investigated controller is also presented by implementing a discrete time realization of the control algorithm using digital controller interfaced in real time with MATLAB®/Simulink®. The hardware results are elucidated. The feasibility of the proposed controller is theoretically and experimentally verified by its efficiency compared to the classical techniques, the available tunable parameters in the controller structure and the immense flexibility in the attainable closed loop dynamics.**

Keywords-intelligent compensator; customized programmed PWM; rapid control prototyping; pure sine wave inverter; isolation power supplies; digital controller; intelligent controller

I. INTRODUCTION

A switch-mode-dc-to-ac inverters are fundamental to motor drives and uninterruptible power supply circuits. Their significance is well manifested by their key importance in the modern era applications like grid tied inverters, the balance of system (BoS) solar inverters, induction heating coil inverters, high-voltage direct current (HVDC) station inverters etc.[1]. There are various types of inverter implementation topologies and gate drive mechanism in practice these days. The most familiar form is the pulse width modulation (PWM) inverter. The availability of the cheap, fast and reliable digital microprocessors has increased the domain of application for the PWM inverters owing to the advent of Digital Pulse Width Modulated (DPWM) drive techniques, in contrast to the classic methods that rely heavily on analog electronics for instance classical Sinusoidal PWM (SPWM) scheme. Various different techniques have been proposed for gate drive and inverter implementation topologies with the objectives of achieving increased power efficiency and reduced harmonic loss [2], for instance, the performance analysis of different control strategies in a z-source inverter in investigated in [3]. A three-phase three-level voltage source inverter with a three-phase two-level inverter as a main circuit is presented in [4]. The performance of random PWM controlled converters is analyzed in [5]. The Programmed PWM (PPWM) techniques to eliminate harmonics have been evaluated in [6]. However, a clear power efficiency comparison of PPWM techniques with traditional techniques like the SPWM technique is not explicitly present in the literature. The digital modules that are used to generate PPWM waveforms are programmable hence, they provide extra degrees of freedom that are not possible with conventional analog methods. These programmable processors enable us to generate "customized" PWM waveforms that may optimize the performance indexes such as the current and the voltage selective harmonics elimination or minimization. It, in turn, gives us control on the torque harmonics and the speed ripples. The harmonic loss can also be minimized. We regard such waveforms as custom programmed PWM (CPPWM). We have designed a power efficient sine wave inverter for which we have addressed the problem of CPPWM signals generation. These signals are optimized for the particular harmonic content minimization and the fundamental component maximization. The results are subsequently compared with the results of SPWM technique for power efficiency.

The inverter design is followed by regulation of the output voltage amplitude in response to the source voltage fluctuations and the output current variations resulting from the electrical or electromechanical load variations. There are various feedback control laws that are proposed and tested in the literature, for instance, the direct power control method is presented in [7]. A deadbeat control for three phase PWM inverter using FPGA

based hardware controller is discussed in [8]. An easy, simple, and flexible control scheme for a three-phase grid-tie inverter system is presented in [9]. A variable gain PI controller is implemented in [10]. A direct torque control scheme is presented in [11]. Although these techniques fulfill well the objectives that are present in the respective article, however, we propose the intelligent controller scheme of Figure 1. By introducing an element of the environment (load etc.) and systems' parameter (current, voltages, frequency, faults etc.) monitoring, our algorithm adjusts its parameter to make the system behave as desired. The parameter adjustments capability is implemented by a multi-dimensional look-up-table (LUT) and an if-then-else conditional statement algorithm. This compensation scheme is intuitive, easy to be programmed in the EEPROM for execution by the digital processors, provides flexibility in the control of system behavior and resulted in excellent system transient performance.

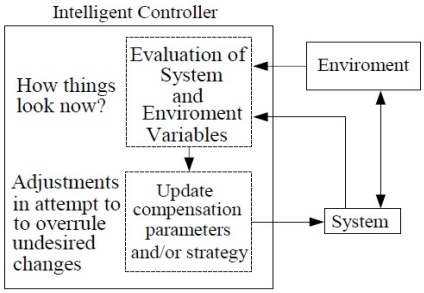

Fig. 1. The schematic block diagram of a general intelligent controller.

II. AN OVERVIEW OF PROPOSED INVERTER SYSTEM

The schematic diagram of the proposed inverter system is shown in Figure 2. A DC-to-AC inverter is driven by a CPPWM module that is interfaced with a PC unit in the Rapid Control Prototyping (RCP) Mode. This mode enables us to monitor and update system parameters during real-time operation of the plant. The inverter drives an electrical or electromechanical load. The DC supply is provided to the inverter from a variable DC supply system, which is implemented by controlled rectification of mains AC supply and low-pass filtering. The sensors are used in the system to monitor currents and voltages at various nodes and branches in the system. An intelligent controller monitors the data from these sensors and controls the DC voltage level to regulate the inverter output voltage.

A supervisory PC-unit in RCP mode is interfaced in real-time with an NI® Data-Acquisition-Card (DAQ), and two Atmel® SAM3X8E ARM Crotex-M3 core digital boards. The DAQ is used for data monitoring from the sensor board. This sensor board comprises of potential transformers (PT) for voltage sensing, Hall-effect sensors for current sensing and signal conditioning network. An induction motor acts as a variable electromechanical load. A tachometer is used to measure the speed of this motor. The controlled variable DC power supply comprises of a controlled thyristor full bridge converter followed by a capacitor bank for removing ripples from rectified output. One of the two digital boards is used to generate the thyristor firing signal. The other digital board is used to generate CPPWM signals to drive the MOSFET board and transformer assembly for DC to AC inversion. The output of the inverter is low pass filtered and drives the electromechanical load. The hardware experimental setup is shown in Figure 4.

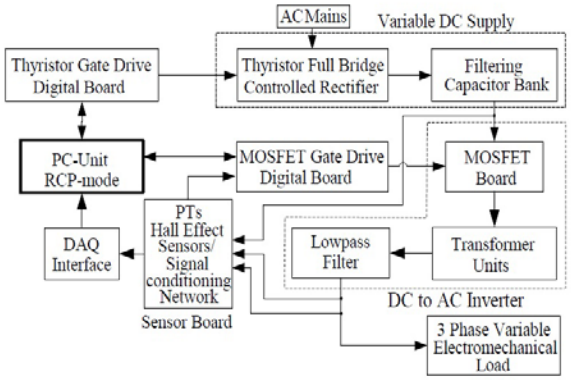

Fig. 2. The schematic block diagram of the proposed inverter system.

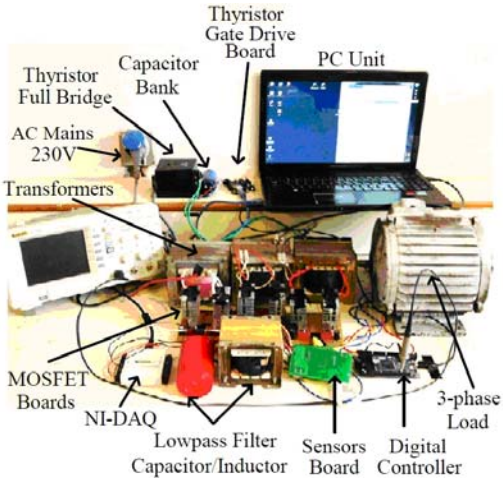

Fig. 3. The hardware experimental setup.

III. THE CUSTOM PROGRAMMED PWM GENERATION PROBLEM

A typical CPPWM waveform is shown in Figure 4. It has quarter wave symmetry hence the waveform generation problem is formulated for the interval $[0, \pi/2]$. This interval is broken down into N points at the angles β_i such that starting from an initial waveform value of 0, waveform toggles at point until we reach at $\pi/2$, hence these angular variables β_i are pulse toggling angles such that,

$$0 < \beta_k < \beta_{k+1} < \frac{\pi}{2},\ k \in [1, N] \qquad (1)$$

We want a customized waveform of Figure 4 such that the amplitude of its fundamental component is maximized and the amplitudes of subsequent selective harmonics are minimized.

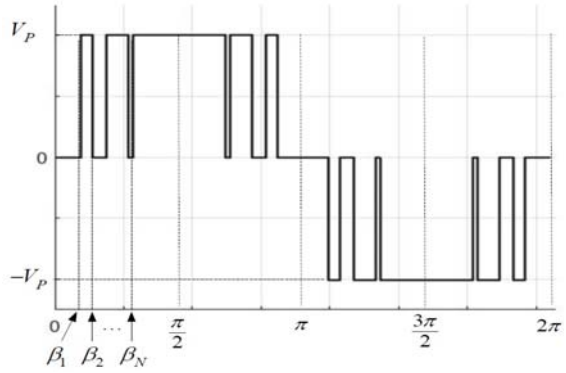

Fig. 4. A general CPPWM waveform demonstrating the pulse toggle angles β_i's and the quarter wave symmetry.

The CPPWM generation problem boils down to the problem of determination of angular variables under the constraints of maximization of fundamental amplitude and elimination of subsequent selective harmonics from the Fourier contents of CPPWM. This is an optimization problem. To eliminate m harmonics and to control the amplitude of fundamental, we must have $N=m+1$ angular variables Resulting equations are nonlinear transcendental with a non-unique solution. Since the CCPWM waveform has quarter symmetry and it is an odd function so it has only odd harmonics [12] given by,

$$b_n = \frac{4}{n\pi}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\beta_k),\quad n\in\{1,3,5,\cdots\} \qquad (2)$$

We select to maximize the fundamental b_1 and to eliminate first consecutive 7 odd harmonics hence, we have m=7 and $N=8$ in (2). The corresponding optimization problem can be formularized as,

$$\max_{\beta} b_1 = \frac{4}{\pi}\sum_{k=1}^{8}(-1)^{k+1}\cos(\beta_k) \qquad (3)$$

Subjected to equality and inequality constraints,

$$b_n = \frac{4}{n\pi}\sum_{k=1}^{8}(-1)^{k+1}\cos(n\beta_k) = 0 \qquad (4)$$

$$0 < \beta_k < \frac{\pi}{2}$$

$$n\in\{3,5,7,9,11,13,15\}$$

These equality constraints in (4) can be written in the matrix notation as $\mathbf{M}=\mathbf{0}$. Now considering the defining $c(.) \triangleq \cos(.)$ the matrix $\mathbf{M}$ is given by (5). The optimization problem formulated for CPPWM generation is solved using the optimization toolbox of MATLAB™. The resulting values of the CPPWM waveform toggle angles are given in Table I.

TABLE I. CPPWM WAVEFORM PULSE TOGGLE ANGLES β_i

PWM Waveform Toggle angles	Values (deg)	Toggle time (msec)
β_1	13.8055	0.7670
β_2	21.3150	1.1842
β_3	27.9059	1.5503
β_4	58.4557	3.2475
β_5	63.9416	3.5523
β_6	75.9398	4.2189
β_7	85.0347	4.7242
β_8	89.7661	4.9870

$$\begin{bmatrix} c(3\beta_1) & -c(3\beta_2) & c(3\beta_3) & -c(3\beta_4) & c(3\beta_5) & -c(3\beta_6) & c(3\beta_7) & -c(3\beta_8) \\ c(5\beta_1) & -c(5\beta_2) & c(5\beta_3) & -c(5\beta_4) & c(5\beta_5) & -c(5\beta_6) & c(5\beta_7) & -c(5\beta_8) \\ c(7\beta_1) & -c(7\beta_2) & c(7\beta_3) & -c(7\beta_4) & c(7\beta_5) & -c(7\beta_6) & c(7\beta_7) & -c(7\beta_8) \\ c(9\beta_1) & -c(9\beta_2) & c(9\beta_3) & -c(9\beta_4) & c(9\beta_5) & -c(9\beta_6) & c(9\beta_7) & -c(9\beta_8) \\ c(11\beta_1) & -c(11\beta_2) & c(11\beta_3) & -c(11\beta_4) & c(11\beta_5) & -c(11\beta_6) & c(11\beta_7) & -c(11\beta_8) \\ c(13\beta_1) & -c(13\beta_2) & c(13\beta_3) & -c(13\beta_4) & c(13\beta_5) & -c(13\beta_6) & c(13\beta_7) & -c(13\beta_8) \\ c(15\beta_1) & -c(15\beta_2) & c(15\beta_3) & -c(15\beta_4) & c(15\beta_5) & -c(15\beta_6) & c(15\beta_7) & -c(15\beta_8) \end{bmatrix} \qquad (5)$$

Using (2) the normalized harmonic amplitude can be expressed by (6).

$$h_{bn} = \frac{b_n}{\left(4V_p/\pi\right)} = \frac{1}{n}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\beta_k) \qquad (6)$$

$$n\in\{1,3,5,\cdots\}$$

Figure 5 shows the comparison of harmonics contents from (6) for CPPWM and SPWM with frequency modulation ratio $m_f = 40$ and amplitude modulation ratio $m_a = 0.8$ [1]. This comparison plot is further explored in section IV.

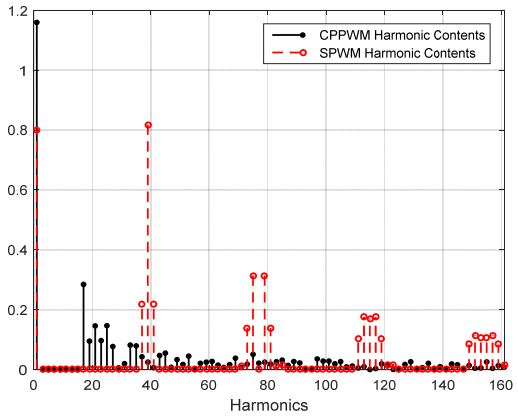

Fig. 5. Comparison of harmonic contents of CCPWM scheme and SPWM scheme.

IV. THE POWER EFFICIENCY CONSIDERATIONS FOR CPPWM SCHEME

A. The Runnig Switching Energy Loss (RSEL)

The instantaneous switching power loss $p_s(t)$ for a typical MOSFET is plotted in Figure 8 for a resistive load I_o and the drain voltage V_d. The turn on time $t_{c(on)}$ and turn off time $t_{c(off)}$ for a typical MOSFET are given by (7) and (8).

$$t_{c(on)} = t_{delay(on)} + t_{rise} \quad (7)$$

$$t_{c(off)} = t_{delay(off)} + t_{fall} \quad (8)$$

The parameters rise time t_{rise}, fall time t_{fall}, on delay time $t_{delay(on)}$ and off delay time $t_{delay(off)}$ in (7)-(8) can be determined from the manufacturer's datasheet for a particular MOSFET unit.

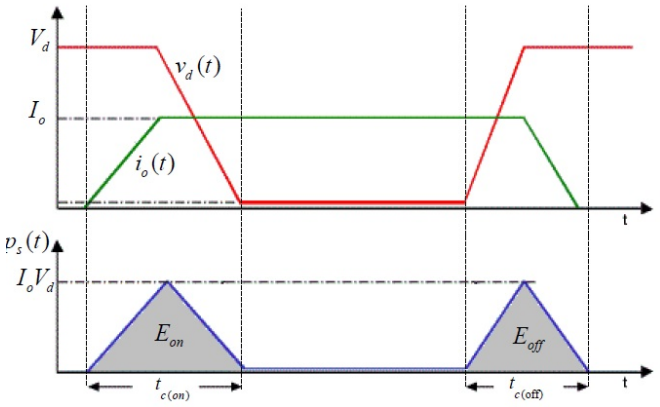

Fig. 6. Demonstration of MOSFET switching power losses.

The Running Switching Energy Loss (RSEL) is defined in (9) as a comparison criteria for energy and power efficiency of different PWM schemes.

$$e_{rsel}(t) = \int_0^t p_s(t)d\tau = n_{\uparrow}(t)E_{on} + n_{\downarrow}(t)E_{off}$$

$$= n_{\uparrow}(t)\frac{1}{2}V_dI_ot_{c(on)} + n_{\downarrow}(t)\frac{1}{2}V_dI_ot_{c(off)} \quad (9)$$

In (9) $n_{\uparrow}(t)$ and $n_{\downarrow}(t)$ are the number of positive edges and the number of negative edges in the PWM waveform from time 0 to t respectively. E_{on} and E_{off} are the areas of shaded regions in Figure 8. Noting the fact that typically $t_{c(on)} = t_{c(off)} = t_c$, we can recast (9) to describe the normalized RSEL $e_{nrsel}(t)$ in (10). The plot for comparison of $e_{nrsel}(t)$ for SPWM and CPPWM schemes is shown in Figure 8. A reduction of nearly 58% in switching losses is clearly visible.

$$e_{nrsel}(t) = \frac{e_s(t)}{0.5V_dI_ot_c} = n_{\uparrow}(t) + n_{\downarrow}(t) \quad (10)$$

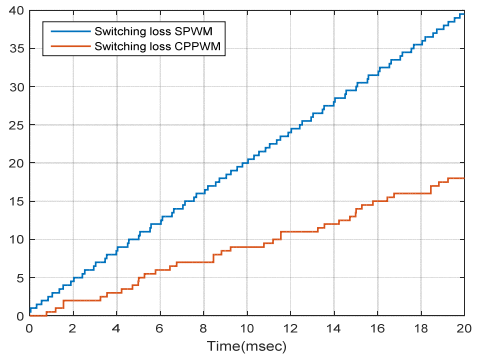

Fig. 7. Comparison of the normalized RSEL for the SPWM and CPPWM schemes over one cycle of the waveform.

B. The Receding Harmonic Energy Loss(RHEL)

The Receding Harmonic Energy Loss (RHEL) is defined in (11) as a comparison criteria for energy and power efficiency of different PWM schemes.

$$E_{h_x}[n_i] = \sum_{k=n_i}^{n_N} \left(h_x[k]\right)^2 \quad (11)$$

The physical interpretation of $E_{hx}[n_i]$ is that it is a measure of the sum of energy of Fourier components in the discrete interval $[n_i, n_N]$. The plot of (11) for the SPWM and CPPWM schemes for $N = 161$ is shown in Figure 8.

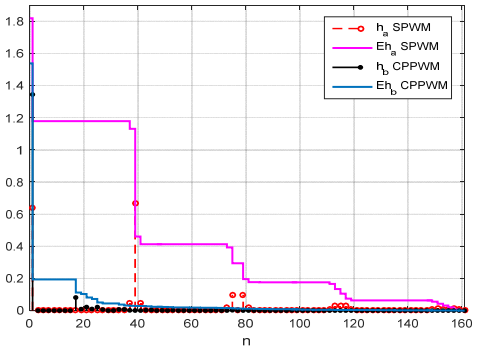

Fig. 8. Plot of the Receding Harmonic Energy Loss (RHEL) for the harmonic contents of SPWM and CCPWM schemes; a manifestation of filtering energy loss.

If a filter is chosen with a cutoff frequency $f_c \in (10f_F, 20f_F)$, where f_F is the fundamental frequency, then it is evident from Figure 8 that by using CPPWM scheme there is nearly 83% reduction in the energy

consumed by the low-pass filter that will not be able to reach the load and hence a significant reduction in the filtering energy loss.

V. INTELLIGENT COMPENSATOR FOR OUTPUT VOLTAGE REGULATION

The implementation of the feedback mechanism for output voltage regulation in response to the variations of load current and voltage is shown in Figure 9.

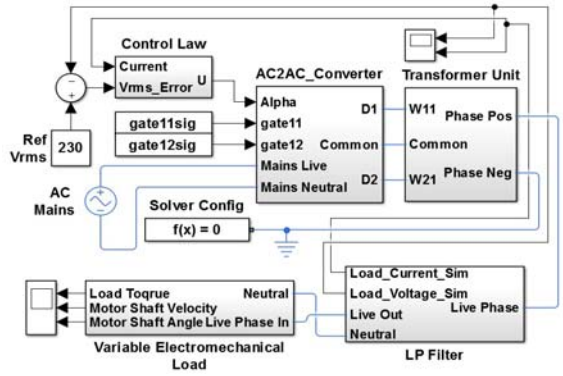

Fig. 9. Simulink model of the single phase sine wave inverter with the voltage regulation feedback mechanism.

The AC-to-AC converter block in Figure 9 consists of the two dotted boundary modules in Figure 2, namely variable DC supply and DC-to-AC inverter. Its expanded view is shown in Figure 10.

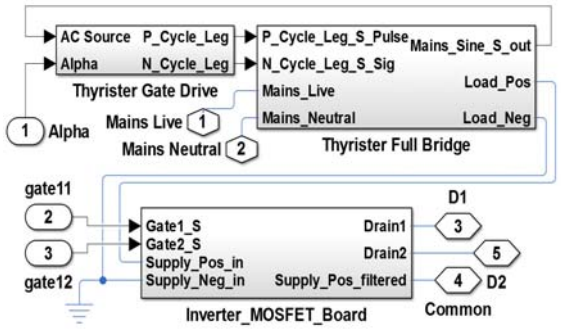

Fig. 10. Expanded view of the AC-to-AC subsystem.

The thyristor gate drive subsystem produces firing pulses for the controlled full bridge thyristor circuit. It takes the firing angle command in degrees as an input from the controller block. Figure 11 shows the inverter topology that been implemented to eliminated the need of multiple isolation power supplies in contrast to the half bridge and the full bridge inverter topologies [1]. The CPPWM sequence shown in Figure 4 is broken down into two sequences to drive MOSFETs in the two branch inverter topology of Figure 11. These two sequences are shown in Figure 12. A single isolation power supply for the gate drive of MOSFET board is needed.

The cutoff frequency for the low pass filter in Figure 9 is set at 500Hz. A variable electromechanical load subsystem is designed to test the control algorithm against load variations in the simulation. The control law subsystem in Figure 9 is shown expanded in Figure 13. It monitors the RMS value of load voltage error and load current and produces the firing angle as its output to adjust the variable DC power supply output that in turn drives MOSFET board and connected with it the transformer unit. The intelligence in the control law has been implemented using a cascade of two parts. The first part consists of a 2-Dimensional Look Up Table (2D-LUT) followed by the second part with consists of if-then-else conditional algorithm.

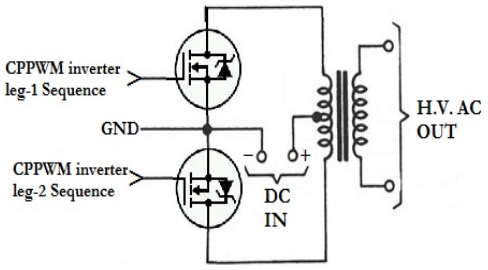

Fig. 11. Two branch inverter topology.

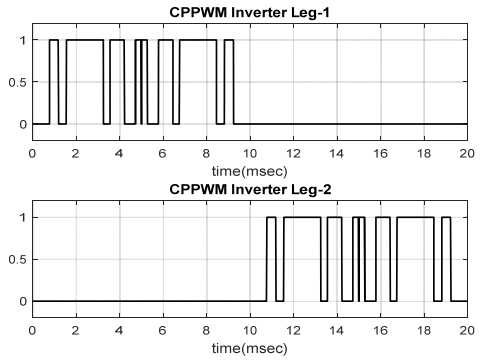

Fig. 12. Decomposition of CPPWM sequence into two unipolar waveforms for the single phase inverter.

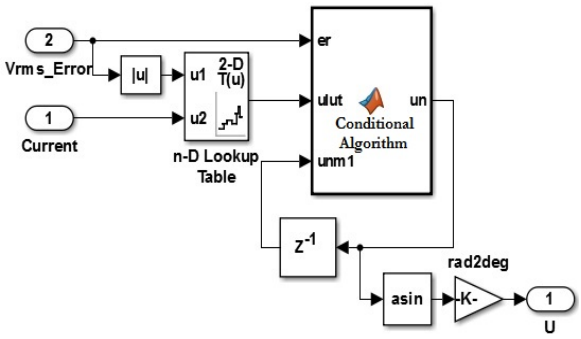

Fig. 13. Expanded view of the control law subsystem.

The LUT part makes a decision on the value of the variable $u_{LUT}[n]$ on the basis of RMS load voltage error $V_{RMS\ Error}[n]$ and load current $I_L[n]$. The variable $u_{LUT}[n]$ represents proposed change to be made in the value of the firing angle $u[n]$. The LUT values are online tuned in MATLAB using Rapid Control Prototyping (RCP) mode of operation. The selection of the value of $u_{LUT}[n]$ by LUT is represented by the surface-mesh plot in Figure 14.

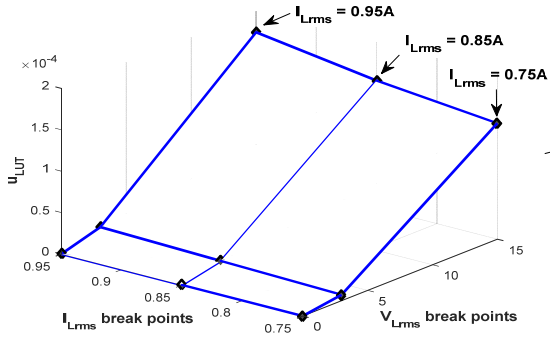

Fig. 14. Surface (mesh) based depiction of the proposed 2-D LUT data.

The second part of the intelligent control law takes in the value of the incremental variable $u_{LUT}[n]$ and $V_{RMS\ Error}[n]$, and makes decision on the value of the variable $u_{sat}[n]$ that is the firing angle in radian. The flow chart of this conditional algorithm is shown in Figure 15.

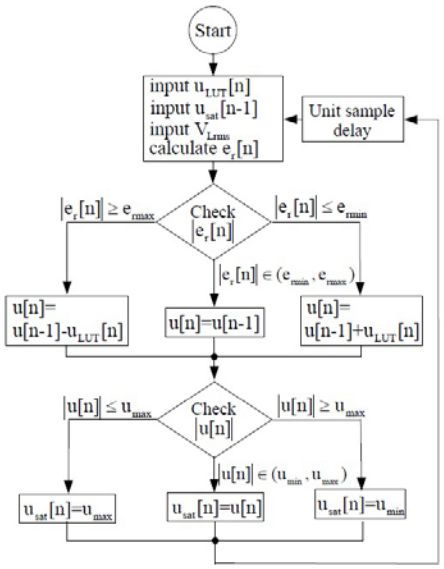

Fig. 15. Flow chart based explanation of the functionality of Code-Based-Algorithm (CBA) block.

The *max* and *min* values in the flowchart are online tuned using RCP mode of operation of the system. These values are given by,

$$e_{\min} = -5, \quad e_{\max} = 5, \quad u_{\min} = 0, \quad u_{\max} = 0.98 \qquad (12)$$

The implementation of a three-phase inverter system supplying a star connected electrical load is shown in Figure 16. The CPPWM signals for inverter unit 2 and unit 3 are simply 120° and 240° phase shifted (time delayed) versions of sequences shown in Figure 12 respectively.

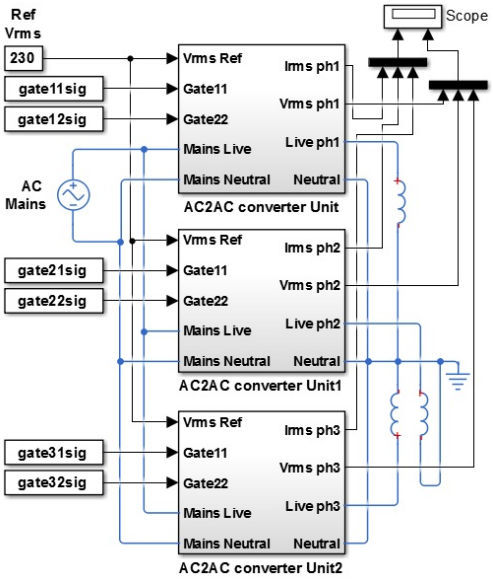

Fig. 16. Extension of the single phase inverter to the three phase implementation

VI. RESULTS

Figure 17 shows the step response of the variable DC power supply module output voltage for two different output load current conditions. The responses are stable and have settled down in 1sec with the overshoot or undershoot not greater than 12%.

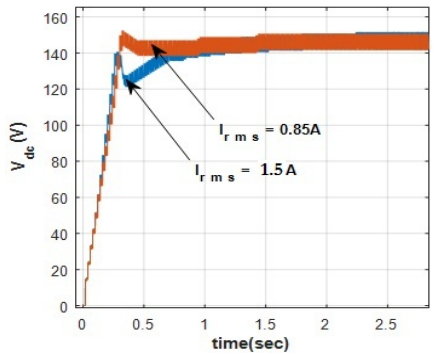

Fig. 17. Step responses of DC voltage for the two different output load current conditions.

Figure 18 shows the step response of the variable DC power supply module output current. The response is stable and has settled down in 0.5 sec with an overshoot of 4%. Figure 19 shows the step response of RMS value of the load voltage for two different output load current conditions. The responses are stable and have settled down in less than 1sec time within a settling band of 5% and the overshoot or undershoot not greater than 7%.

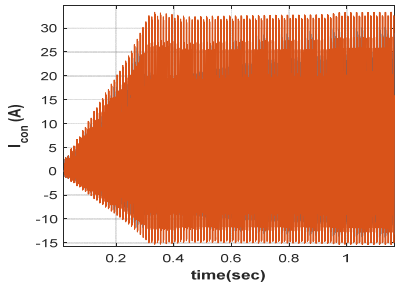

Fig. 18. Step response for the variable DC power supply output current.

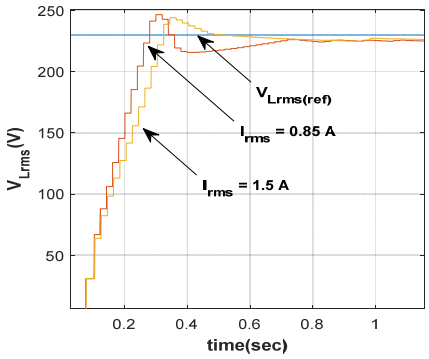

Fig. 19. Simulation step responses for the load voltage RMS value for two different output load current conditions.

Figure 20 shows the step response of RMS value of the load current for two different output electrical conditions. The responses are stable and have settled down in less than 5 sec.

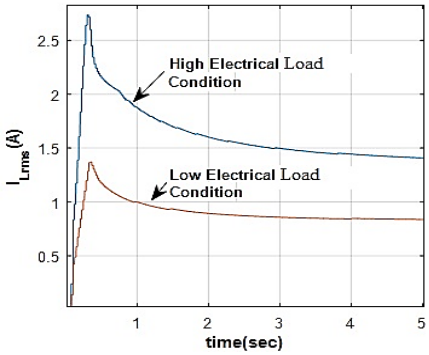

Fig. 20. Simulation responses for the load current RMS value: Step responses for the two different output electrical load conditions.

Figure 21 shows the experimental step response of the instantaneous value of the load voltage. The response is stable and has settled down in less than 0.65 sec time within a settling band of 5% and the overshoot less than 6%. Figure 22 shows the experimental step response of the instantaneous value of the load current. The response is stable and has settled down in less than 3.5 sec time within a settling band of 5%.

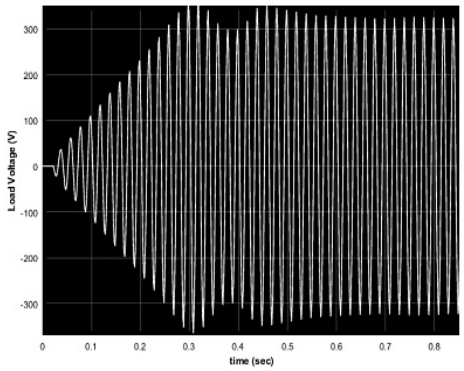

Fig. 21. Experimental responses for the instantaneous load voltage.

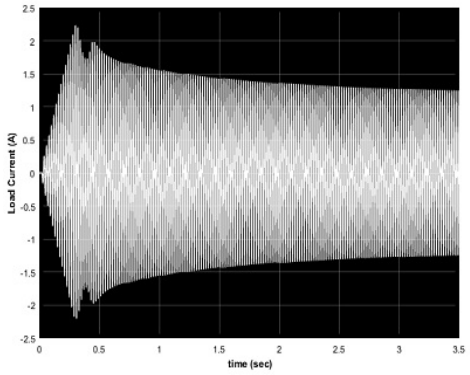

Fig. 22. Experimental responses for the instantaneous load current.

VII. DISCUSSION AND CONCLUSION

A power efficient inverter system with intelligent controller algorithm to regulate the output voltage in response to load and input variations has been presented. A custom programmed PWM scheme has been implemented with an objective of optimal selective harmonic elimination and maximization of the fundamental. As compared with a special case of SPWM our results show a promising 58% reduction in switching losses and about 83% reduction in the filtering energy loss. Analysis can be further extended for comparison with the SPWM scheme with different amplitude and frequency modulation ratios and the other PWM schemes like vector-space PWM. An inverter electronic topology has been implemented that does not require multiple isolation power supplies for the gate drive. An intelligent controller scheme has been implemented. The voltage regulation results are satisfactory and system withstands load variations and various disturbances within admissible stability and performance margins.

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