A Five-Level Current-Source Inverter for Grid-Connected or High-Power Three-Phase Wound-Field Synchronous Motor Drives

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***Abstract*—Simple converter structure, inherent short-circuit protection and regenerative capability are the most important advantages of current-source inverters (CSI's) which have made them suitable for medium-voltage high-power drives. Usually in grid-connected gas turbine generators or pumped storage hydro power plants, efficient and reliable current-source load-commutated inverters (LCI's) with thyristor switches are employed. Also, this type of CSI is widely used in very large drives with power ratings of tens of megawatts to supply wound-field synchronous motors (WFSM's). However, LCI's suffer from some disadvantages such as large torque pulsations, poor power factor, and start-up criticalities. In this paper, a novel multilevel-based CSI is proposed. The proposed converter consists of one LCI and one CSI bridge with self-turn-off switches along with a voltage clamping circuit. The CSI switches are forced commutated; hence, a voltage clamping circuit is employed to limit voltage spikes caused by current variations in inductive paths during commutation transients. Drastic reduction in harmonic distortion of stator current and improved fundamental power factor are achieved by the proposed topology. In addition, torque pulsations are reduced remarkably for normal and starting operating conditions. Comprehensive analysis of the proposed structure is presented and the design of converter components is elaborated.**

Keywords-current-source inverter (CSI); five-level current waveform; load-commutated inverter (LCI); voltage clamping circuit; wound-field synchronous motor (WFSM) drive

I. INTRODUCTION

In industrial current-source inverter (CSI)-fed drives, self-turn-off power devices such as gate turn-off thyristors (GTO's) or insulated gate bipolar transistors (IGBT's) are switched by pulsed-width modulation (PWM) schemes such as trapezoidal PWM (TPWM), selective harmonic elimination (SHE) and space vector modulation (SVM) to attenuate the low-frequency harmonic components of the machine stator current [1]1-3]. In these structures, a three-phase capacitor bank is mandatory at the CSI output to absorb the high-voltage spikes produced due to the switching of the current in inductive paths. The capacitor bank also serves as a filter for high-frequency current harmonics created by the PWM switching. However, this capacitor bank has some drawbacks such as the possibility of the resonance risk between output capacitors and machine magnetizing inductance at the fundamental frequency or machine leakage inductance at higher harmonic orders [4]. Thus, the capacitor bank must be designed so that the lowest harmonic order of the stator current is much higher than the resonance frequency. Accordingly, the bank size will typically range between 0.3 per unit (pu) to 0.5 pu for switching frequencies of approximately 400 Hz [1]. Furthermore, the effect of the capacitor bank on the motor current and air-gap flux specifically at high operating speeds must be taken into account in the control system so as to get adequate response and avoid instability of the drive at transients [5].

In addition to these disadvantages, for some high-power applications (usually higher than 10 megawatts [6]) using PWM switching is not usual in CSI-fed drives since the converter efficiency is reduced due to the switching and conduction losses of the self-turn-off power devices. Therefore, load-commutated inverter (LCI)-fed wound-field synchronous motor (WFSM) drives are the preferred choice in this power range because of the higher efficiency and reliability of the converter. Also, the initial investment cost of the converter is low due to the inexpensive silicon-controlled rectifier (SCR) devices [1]. In these drives, WFSM operates at over-exciting mode resulting in natural commutation of the thyristors [7]. Therefore, there is no need for capacitor banks.

LCI-fed drives are widely used in high-power applications specifically in pumped-storage power plants and gird-connected synchronous machines for star-up purposes [8, 9]. Due to the great increase in social electricity consumption level and the proliferation of the capacity of nuclear power and renewable energy resources, it was expected that the capacity of pumped-storage power plants would gain more than 200 GW worldwide by 2014 [10, 11]. There is also a great trend in utilizing LCI's for driving high-power compressors used for liquefying natural gas, pumps, fans [12-14], grinding mills in mining applications [15] and ship propulsion systems [1].

However, the quasi-square waveform of the stator phase current of these drives is a major problem. This waveform is rich in low order harmonics, specifically 5th and 7th orders, which result in large torque pulsations and increased winding and iron losses. The torque ripples can interact with the torsional natural frequencies (TNF's) of the mechanical system and lead to accelerated shaft fatigue, lifetime reduction, gear-box damage, and system failures [12-14]. The most common method to reduce the torque pulsations is to use dual three-phase WFSM in which each three-phase winding set of the machine is independently supplied from a three-phase LCI [6, 16]. In this configuration, the 6th order of the electromagnetic torque is cancelled out. Although, this solution is not always possible, e.g. it does not cover the cases where LCI's are utilized to feed grid-connected (three-phase) generators for start-up before synchronization or in pumped storage hydro power plants [7]. Another solution is to use multi-pulse converters. In these structures, two series or paralleled 6-pulse (three-phase) LCI's are connected to a three-phase three-winding phase-shifting transformer feeding a three-phase WFSM to eliminate the 6th order harmonic of the torque. However, the transformer is bulky and expensive and increases system losses [17]. On the other hand, recent development in in high-power semiconductor devices such as IGBT's has drawn the attention to use voltage-source inverters (VSI's) in these applications. In [11], a multilevel cascaded H-bridge (CHB) VSI is used for the start-up of synchronous motor in a pumped storage power station. In this configuration the harmonic distortion of the stator current is improved remarkably, however, the volume of the converter is increased since there are nine power cells connected in series each phase.

Another problem regarding to LCI-fed WFSM drives is the start-up operating conditions. At standstill or low speeds, the generated back electro-motive forces (EMF's) of the machine are not large enough to turn off thyristors and the load commutation process, as will be explained in III.*A*, is not accomplished. To cope with this problem, dc-link pulsing method is generally used [7, 18]. In this method, the dc-link current is forced to zero by the operation of the rectifier at the commutation instants. Therefore, the previous conducting thyristors in the LCI is turned off since its current reaches below the holding current [19, 20]. After a short interval, the next incoming thyristor is fired and the dc-link current is again built up to its reference value by the rectifier. However, this method produces high torque ripples.

In this paper, a novel multi-objective structure for LCI-fed three-phase WFSM's is proposed based on the five-level current-source configuration. In addition to several advantages related to high-power multilevel converters such as reduction of the voltage and current stresses of the switching devices and lower harmonic distortion of the load current [21][21], the machine fundamental power factor is improved significantly. Furthermore, the start-up criticalities of the LCI-fed WFSM drives are removed with the proposed structure.

II. STRUCTURE OF THE PROPOSED FIVE-LEVEL CONVERTER

The proposed five-level converter is shown in Figure 1 and consists of two converters (that supply the main power of WFSM): an LCI with thyristors T_1-T_6 and a CSI with self-turn-off power devices S_1-S_6. In CSI-fed WFSM drives, each motor phase can be modeled as a sinusoidal back EMF in series with the commutation inductance, L_C, which is approximately equal to $(L''_d+L''_q)/2$ [19], as shown in Figure 1. L''_d and L''_q are the machine sub-transient inductances along rotor *d* and *q* axes, respectively. It should be mentioned that stator resistances are neglected in this circuit.

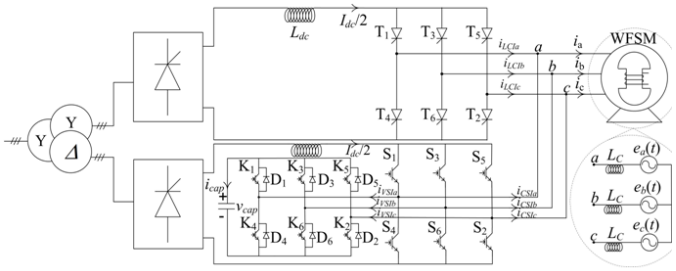

Fig. 1. Proposed five-level CSI for WFSM drives.

Both converters are switched at the machine fundamental frequency. Since the CSI switches are forced-commutated, the variation rate of current in machine inductances must be limited at the commutation transients. On the other hand, the capacitor bank cannot be utilized because its size would be very large due to the low switching frequency of the converters. In this paper, a voltage clamping circuit is used to inhibit voltage spikes. Voltage clamping circuits usually consist of a diode rectifier to transfer the reactive energy of the machine to an electrolytic capacitor at the commutation intervals [21]. In order to avoid the continuous increment of the capacitor voltage, an energy recovery circuit such as a DC/DC chopper or an inverter is used to pump the capacitor energy into the dc-link or ac-grid, respectively [21].

In this paper, a voltage-source inverter (VSI) is utilized with six self-turn-off devices K_1-K_6 and six free-wheeling diodes D_1-D_6 as shown in Figure 1. The same VSI is introduced in [22] to reduce voltage spikes in a thyristor-based CSI-fed induction motor drive. In [22], the VSI is employed for two main tasks: 1) forced-commutation of the thyristors and 2) clamping the voltage spikes. While, the VSI in the proposed multilevel converter serves only as the voltage clamping circuit during commutation transients and thyristors are turned off naturally. For this reason, as will be explained in Section III.*B*, the conduction states of the switches in the proposed multilevel are different and simpler than those presented in [22].

III. OPERATION PRINCIPLES OF THE PROPOSED FIVE-LEVEL CONVERTER

The desired stator phase current waveform, e.g. $i_a(t)$ in Figure 1, of the proposed five-level converter is shown in Figure 2a. This waveform results from the summation of two quasi-square waveforms, i.e. $i_{LCIa}(t)$ and $i_{CSIa}(t)$, at node *a*

(Figure 1). As in the case of conventional LCI's, $i_{LCIa}(t)$ and $i_{CSIa}(t)$ have a pulse-width of 120 electrical degrees in each half cycle and $i_{LCIa}(t)$ leads $i_{CSIa}(t)$ by 30°. The resultant waveform of $i_a(t)=i_{LCIa}(t)+i_{CSIa}(t)$ has five levels of 0, $\pm I_{dc}/2$ and $\pm I_{dc}$.

The phase displacement between i_{LCIa} and i_{CSIa}, i.e. $\omega\Delta t$ where ω is the motor speed in electrical rad/sec, is set to 30° so as to minimize the THD of i_a as shown in Figure 2b. According to this figure, the amplitude of the 5th and 7th harmonic components of the desired phase current is equal to 5.36% and 3.83% of the fundamental for $\omega\Delta t$=30°, respectively, while they would be 20% and 14.35% if the usual LCI topology with quasi square-wave currents were employed.

A. Operation principles of LCI

The switching pattern for the LCI thyristors is shown in Figure 3. Since the thyristors of the LCI are naturally commutated, currents $i_{LCIa}(t)$, $i_{LCIb}(t)$ and $i_{LCIc}(t)$ must lead the phase voltages $e_a(t)$, $e_b(t)$ and $e_c(t)$ with a minimum angle of $\varphi_{LCImin}=\mu+\omega t_q$ [19], where μ is the commutation angle and t_q is thyristors turn-off time.

Considering phase '*a*' as an illustration, practically negative and positive zero-crossing instants of $e_{ac}(t)$ are used as the reference for firing T_1 and T_4, respectively. Thus defining α as the firing angle, T_1 will be fired at point A in Figure 2a and the commutation interval '1', shown in Figure 3, is started. Conduction of T_1 produces a short-circuit loop between the incoming phase '*a*' and the outgoing phase '*c*' as shown in Figure 4 in which $e_{ac}(t)$ drives $i_{LCIc}(t)$ to decrease from $I_{dc}/2$ to 0 and $i_{LCIa}(t)$ to increase from 0 to $I_{dc}/2$. The current variations are almost linear since the stator phase resistances are practically negligible. The commutation phenomenon lasts for μ electrical degrees. Consequently, the current in T_5 is diminished to zero and the commutation interval is finished. After commutation, the voltage across T_5 ($e_{ac}(t)$ in this case) must be negative for a time interval of at least equal to t_q in order to be able to withstand positive voltages [20].

Usually in high-power LCI-fed drives the maximum firing angle is set to 150° to avoid commutation failure. In this case, the fundamental component of the current leads stator phase voltage by φ_{LCI} =30°. It should be mentioned that in a conventional three-phase three-level LCI (with levels of 0, $+I_{dc}$ and $-I_{dc}$ in the output waveform of phase current), the fundamental power factor angle, φ_{LCI}, is equal to $\pi-\alpha$. At higher loading conditions, the firing angle is lower than 150° which can be translated into a relatively high reactive power.

B. Operation principles of CSI and VSI

The switching instants and sequences for S1-S6 are the same as T_1-T_6 except for a 30° displacement as shown in Figure 5. For instance, S_1 must be switched on at point B (Figure 2a) which is 30° later than the firing instant of T_1.

Contrary to the situation explained for LCI at point A, the voltage $e_{ac}(t)$ might be positive at point B and, consequently, the current in phase '*c*' cannot be naturally commutated to phase '*a*' by switching of S_1. Therefore, an external negative and positive voltage must be applied to phases '*c*' and '*a*', respectively, to force $i_c(t)$ to decrease from $I_{dc}/2$ to 0 and $i_a(t)$ increase from $I_{dc}/2$ to I_{dc}. In this way, the currents in the outgoing and incoming phases should not abruptly change in order to limit the voltage spikes over the machine inductances. The external voltage source can be a dc capacitor which is applied by proper switching of VSI at commutation instants.

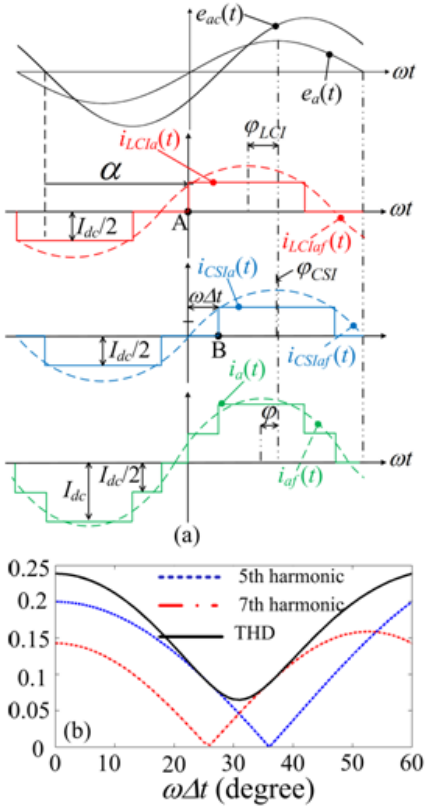

Fig. 2. (a) $i_{LCIa}(t)$, $i_{CSIa}(t)$ and $i_a(t)$ waveforms and their corresponding fundamentals and WFSM phase and line voltages, (b) 5th and 7th harmonic amplitudes (relative to fundamental) and THD for the phase current i_a as a function of $\omega\Delta t$.

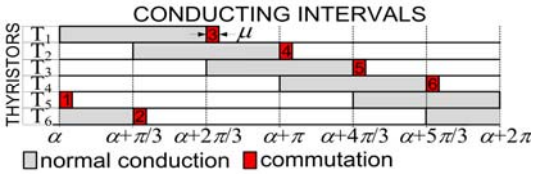

Fig. 3. Switching pattern of LCI. α corresponds to point A in Figure 2a

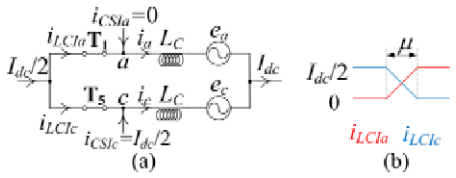

Fig. 4. The loop created by the simultaneous conduction of T_1 and T_5 (commutation interval '1' in Figure 3) and (b) current variations.

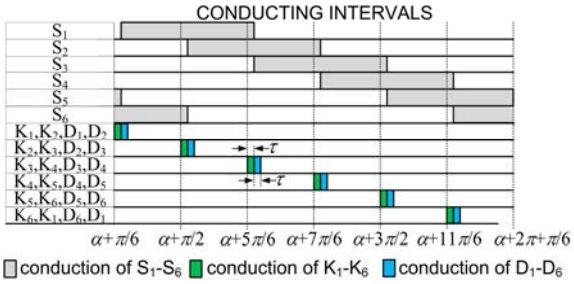

Fig. 5. Switching pattern of CSI and VSI devices. $\alpha+\pi/6$ corresponds to point B in Figure 2a.

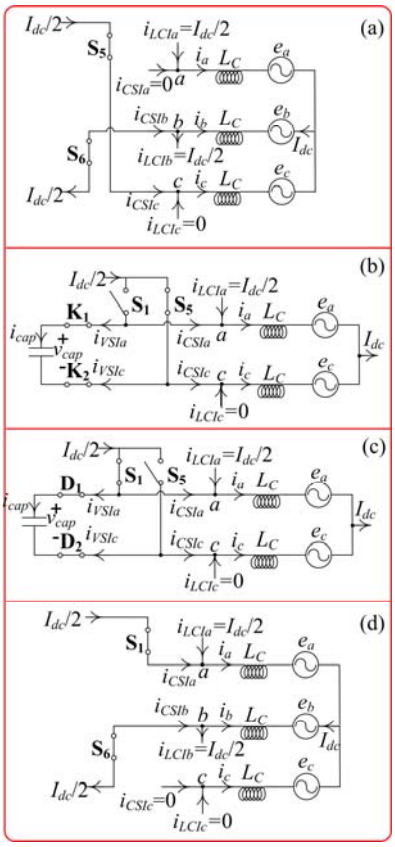

Fig. 6. CSI and VSI equivalent circuits for: (a) normal conduction before commutation between phases '*a*' and '*c*' starts, (b) mode 1, (c) mode 2 and (d) mode 3.

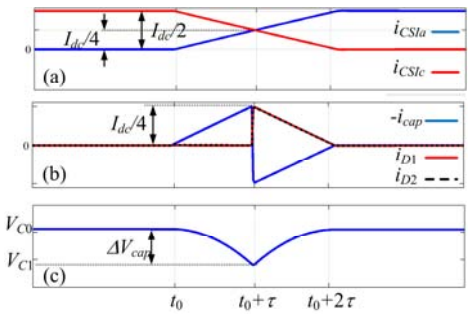

Fig. 7. Waveforms related to commutation between phases '*a*' and '*c*', (a) i_{CSIa} and i_{CSIc}, (b) D_1 and D_2 currents and $-i_{cap}$, (c) v_{cap}.

In order to explain the operation of CSI and VSI at commutation instants, consider switches S_5 and S_6 of the CSI and T_1 and T_6 of the LCI are conducting with the equivalent circuit shown in Figure 6a and S_1 is switched on at $t=t_0$ (point B in Figure 2a). Thanks to the symmetrical operation of the circuit, we confine our analysis to one sixth of a cycle which can be divided into three operating modes. The equivalent circuits of these three modes and their corresponding waveforms are shown in Figs. 6 and 7, respectively.

In the following subsections, details are given on how forced commutation is obtained in the CSI bridge using the VSI. The description includes mathematical details which are however required to obtain some practical dimensioning rules regarding capacitors C_{dc} as well as VSI switches K_1-K_6 and D_1-D_6.

1) Mode 1 ($t_0<t<t_0+\tau$); S_5, S_6, K_1 and K_2 are conducting

At $t=t_0$, K_1 and K_2 are also switched on in addition to S_1. According to the equivalent circuit of this interval shown in Figure 6b and assuming that C_{dc} is initially charged to V_{C0}, capacitor voltage drives i_c and i_{CSIc} ($i_c=i_{CSIc}$) to decrease and i_a and i_{CSIa} ($i_{CSIa}=i_a$-i_{LCIa}) to increase (see Figure 7a). Since the command pulse is not removed from the gate of S_5, the capacitor negative voltage prevents S_1 to conduct. In this period, C_{dc} is discharged ($i_{cap}<0$) via K_1 and K_2 as shown in Figure 7c. By applying Kirchhoff's Voltage Law (KVL) in the loop shown in Figure 6b, one can write:

$$v_{cap} = V_{C0} + \frac{1}{C_{dc}}\int_{t_0} i_{cap}\,dt = L_C\frac{di_a}{dt} + e_a - e_c - L_C\frac{di_c}{dt} \quad (1)$$

and:

$$i_a + i_c = -i_b = I_{dc} \Rightarrow \frac{di_a}{dt} = -\frac{di_c}{dt}$$
$$i_{cap} = i_{VSIc} = -i_{VSIa} = -i_{CSIa} = -i_a + \frac{I_{dc}}{2} \quad (2)$$

In the above equations, $e_a(t)=\sqrt{2}E\sin(\omega t)$ and $e_c(t)=\sqrt{2}E\sin(\omega t-4\pi/3)$ where E and ω are the rms value of the machine back EMF's and machine speed in electrical rad/sec, respectively.

Replacing (2) into (1) and making its derivative yields:

$$2L_C C_{dc}\frac{d^2 i_a}{dt^2} + i_a = C_{dc}\frac{d(e_c - e_a)}{dt} + \frac{I_{dc}}{2} =$$
$$= -\sqrt{6}EC_{dc}\omega\sin(\omega t + \frac{\pi}{3}) + \frac{I_{dc}}{2} \quad (3)$$

Since the inductance current and capacitor voltage cannot go any discontinuity, their value must be equal for $t=t_0^-$ and $t=t_0^+$. Thus, i_a is equal to $I_{dc}/2$ for $t=t_0^+$. Also, C_{dc} is charged to V_{C0} at $t=t_0^-$ and, consequently, the initial condition for the derivative of i_a is obtained according to (1) as:

$$\left.\frac{di_a}{dt}\right|_{t=t_0^+} = \frac{V_{C0} - (e_a - e_c)\big|_{t=t_0}}{2L_C} = \frac{V_{C0} + \sqrt{6}E\cos(\omega t_0 + \frac{\pi}{3})}{2L_C} \quad (4)$$

According to these initial conditions, the final expression:

for $i_a(t)$ in (3) is:

$$i_a(t)=\frac{\sqrt{6}EC_{dc}\omega}{1-(\omega/\omega')^2}\left[\sin(\omega t_0+\frac{\pi}{3})\cos(\omega'(t-t_0))+\right.$$
$$\left.+\frac{\omega}{\omega'}\cos(\omega t_0+\frac{\pi}{3})\sin(\omega'(t-t_0))-\sin(\omega t+\frac{\pi}{3})\right]$$
$$+\frac{V_{C0}+\sqrt{6}E\cos(\omega t_0+\frac{\pi}{3})}{2L_C}\frac{\sin(\omega'(t-t_0))}{\omega'}+\frac{I_{dc}}{2}\cos(\omega'(t-t_0)) \quad (5)$$

where, $\omega'=1/\sqrt{2L_CC_{dc}}$.

If the variations of $i_a(t)$ during this mode occurs rapidly in relation to the rate of variations of the back EMF's, the expression $e_c(t)$-$e_a(t)$ in (1) and (3) can be treated as a constant equal to its value at $t=t_0$. Therefore, (3) is simplified as:

$$2L_CC_{dc}\frac{d^2i_a}{dt^2}+i_a=\frac{I_{dc}}{2} \quad (6)$$

and the simplified expression for i_a during this mode is determined as:

$$i_a(t)=\frac{V_{C0}+\sqrt{6}E\cos(\omega t_0+\frac{\pi}{3})}{2L_C\omega'}\sin(\omega'(t-t_0))+\frac{I_{dc}}{2} \quad (7)$$

This period ends at $t=t_0+\tau$, where, $t_0+\tau$ is considered as the instant in which $i_a(t)$ is increased to $3I_{dc}/4$ and $i_c(t)$ is decreased to about $I_{dc}/4$. In other words, approximately half of the energy stored in phase '*c*' inductance in addition to a fraction of energy stored in C_{dc} are transformed to phase '*a*' to increase its current from $I_{dc}/2$ to $3I_{dc}/4$.

2) Mode 2 ($t_0+\tau<t<t_0+2\tau$); S_1, S_6, D_1 and D_2 are conducting

At $t=t_0+\tau$, K_1, K_2 and S_5 are switched off and S_1 which has received its gating pulse at $t=t_0$ can now conduct. The equivalent circuit for this interval is shown in Figure 6c. In this period, diodes D_1 and D_2 produce a free-wheeling path to avoid discontinuity in current i_a and i_c as shown in Figure 7b. Therefore, the remaining phase '*c*' inductive energy is gradually discharged into phase '*a*' and C_{dc} and increases i_a and v_{cap} as shown in Figs. 7a and 7c. Since the operation of the circuit is repeated every one-sixth of the motor operating frequency, v_{cap} and i_a reach V_{C0} and I_{dc}, respectively, at the end of this period. Similar to mode 1, KVL equation of (1) holds also for this mode. The only difference is in the VSI currents direction. According to the equivalent circuit shown in Figure 6c, one can write:

$$i_a+i_c=-i_b=I_{dc}\Rightarrow\frac{di_a}{dt}=-\frac{di_c}{dt}$$
$$i_{cap}=i_{VSIa}=-i_{VSIc}=i_{CSIc}=i_c=-i_a+I_{dc} \quad (8)$$

Replacing (8) into (1) and making its derivative yields:

$$2L_CC_{dc}\frac{d^2i_c}{dt^2}+i_a=C_{dc}\frac{d(e_c-e_a)}{dt}+I_{dc}=$$
$$=-\sqrt{6}EC_{dc}\omega\sin(\omega t+\frac{\pi}{3})+I_{dc} \quad (9)$$

For simplicity, we can assume that the i_a increment from $3I_{dc}/4$ to I_{dc} in mode 2 takes the same time as its increment from $I_{dc}/2$ to $3I_{dc}/4$ in mode 1. Therefore, (9) can be solved as in (10) knowing that i_a is equal to $3I_{dc}/4$ at $t=t_0+\tau$ and I_{dc} at $t=t_0+2\tau$.

$$i_a(t)=\frac{1}{\sin(\omega'\tau)}\frac{\sqrt{6}EC_{dc}\omega}{1-(\omega/\omega')^2}\left[-\sin(\omega(t_0+\tau)+\frac{\pi}{3})\sin(\omega'(t-t_0-2\tau))\right.$$
$$\left.+\sin(\omega(t_0+2\tau)+\frac{\pi}{3})\sin(\omega'(t-t_0-\tau))\right]$$
$$-\frac{\sqrt{6}EC_{dc}\omega}{1-(\omega/\omega')^2}\sin(\omega t+\frac{\pi}{3})+\frac{I_{dc}}{4\sin(\omega'\tau)}\sin(\omega'(t-t_0-2\tau))+I_{dc} \quad (10)$$

Similar to (6), $e_c(t)$-$e_a(t)$ can be considered as constant during mode 2 and i_a in (10) can be simplified as:

$$i_a(t)=\frac{I_{dc}}{4}\frac{\sin(\omega'(t-t_0-2\tau))}{\sin(\omega'\tau)}+I_{dc} \quad (11)$$

At $t=t_0+2\tau$, the voltage across C_{dc} is equal to V_{C0} for reasons of symmetry. Accordingly, v_{cap} has the following relation by writing KVL in the loop shown in Figure 6c.

$$v_{cap}\Big|_{t=t_0+2\tau}=\left(2L_C\frac{di_a}{dt}+e_a-e_c\right)\Big|_{t=t_0+2\tau}=V_{C0} \quad (12)$$

Therefore the expression for V_{C0} can be achieved by making derivative of (11) and replacing that into (12):

$$V_{C0}=\frac{2L_CI_{dc}\omega'}{4\sin(\omega'\tau)}-E\sqrt{6}\cos(\omega(t_0+2\tau)+\frac{\pi}{3}) \quad (13)$$

3) Mode 3 ($t_0+2\tau<t<t_0+\pi/3$); S_1 and S_6 are conducting

Commutation transient in the CSI ends when i_{VSIa} and i_{VSIc} diminish to zero and the conducting diodes D_1 and D_2 turn off. The equivalent circuit for this mode is shown in Figure 6d. Thus, all the switches in the VSI will be in the OFF state until the next commutation between phases '*b*' and '*c*' in which S_6 is turned off and S_2 is turned on.

IV. DESIGN CONSIDERATIONS OF THE DEVICE COMPONENTS

In this Section, dimensioning of the VSI components is explained by taking a high-power WFSM, with the specifications listed in Table I, as the load. This machine will be later utilized for simulation studies.

Starting from V_{C0} which is an important factor in dimensioning and cost of the dc-link capacitor, this value is a function of different parameters such as E, I_{dc}, ω, C_{dc} and τ as indicated in (13). However, parameters E, I_{dc} and ω in (13) can be extracted according to the different loading conditions of the machine as explained in [23] in which field-oriented control (FOC) in stator flux reference frame is applied.

Among C_{dc} and τ, only τ can be controlled by the VSI. Hence, we first keep C_{dc} equal to a typical value such as 500

μF to study the effect of τ on V_{C0}. In Figure 8, V_{C0} is plotted as a function of τ under different operating conditions, i.e. different values of I_{dc}, using (13). It is obvious from Figure 8 that for shorter time duration τ, V_{C0} rises significantly. For instance, for rated loads where I_{dc} is around 1400 A, V_{C0} reaches to about 3000 V for τ equal to 10 μsec. As illustrated in Figure 6 for the equivalent circuits of commutation intervals in CSI, V_{C0} is superimposed across load terminals during commutation and is applied across the VSI switches during the non-commutating intervals. Therefore, τ must be set to higher values, e.g. higher than 50 μsec, so that to have reasonable values for V_{C0}.

On the other hand, increasing τ results in a longer conduction period for the VSI devices. As an example, in (14), the equation for the current flowing in K_1 is given. In this equation, it is assumed that the current in K_1 is linearly increased from 0 to $I_{dc}/4$ during the first commutation interval ($\alpha+\pi/6<\omega t<\alpha+\pi/6+\tau$) when turning S_1 on and during the sixth commutation interval ($\alpha+11\pi/6<\omega t<\alpha+11\pi/6+\tau$) when turning S_4 off (see Figure 5).

$$i_{K1}=\begin{cases}\dfrac{I_{dc}}{4}\left(t-t_0\right) & t_0\langle t\langle t_0+\tau\\ \dfrac{I_{dc}}{4}\left(t-t_0-5T/3\right) & t_0\langle t\langle t_0+\tau+5T/3\\ 0 & otherwise\end{cases} \tag{14}$$

where, T is the period of the motor quantities, i.e. voltages and currents. Thus, the rms and average values of the current flowing in the VSI switches can be found according to (14) as in (15).

$$i_{Krms}=\sqrt{\frac{1}{T}\int_T\left(i_{K1}\right)^2dt}=\frac{I_{dc}}{2\sqrt{6}}\sqrt{\frac{\tau}{T}}$$
$$i_{Kave}=\frac{1}{T}\int_T\left(i_{K1}\right)dt=\frac{I_{dc}}{4}\frac{\tau}{T} \tag{15}$$

On the other hand, the dc-link current, $I_{dc}/2$, flows in the main switches (T_1-T_6 and S_1-S_6) for an interval of $T/3$ during a period. Consequently, the rms and average values of the current in the main switches can be simply found equal to $I_{dc}/(2\sqrt{3})$ and $I_{dc}/6$, respectively. Thus, i_{Krms} and i_{Kave} can be normalized to those of the main ones as in (15). In Figures 9a and 9b, i_{Knrms} and i_{Knave} are plotted, respectively, as a function of τ for different values of motor speed ($\omega=2\pi/T$). Figure 9 shows that as τ increases the current rating of switches also increases. However, it can be seen that totally the current ratings of the VSI switches are small compared to those of the main switches. For instance, for motor rated speed (628 rad/sec or 100 Hz) i_{Krms} and i_{Kave} are around 5 and 1.1 percent of the rated current of the main switches, respectively, for τ equal to 100 μsec.

The design criteria for the dc capacitor size C_{dc} is the permissible voltage variations $\Delta V_{dc}=V_{C0}-V_{C1}$ shown in Figure 7c. V_{C1} in Figure 7c is obtained as follows by replacing $t=t_0+\tau$ in (1) and using (2) as:

$$i_{Knrms}=\frac{\frac{I_{dc}}{2\sqrt{6}}\sqrt{\frac{\tau}{T}}}{\frac{I_{dc}}{2\sqrt{3}}}=\sqrt{\frac{\tau}{2T}};\quad i_{Kave}=\frac{\frac{I_{dc}}{4}\frac{\tau}{T}}{\frac{I_{dc}}{6}}=\frac{3}{2}\frac{\tau}{T} \tag{16}$$

Substituting (7) into (16), V_{C1} will be equal to

$$V_{C1}=\left(2L_C\frac{di_a}{dt}+e_a-e_c\right)\Big|_{t=t_0+\tau} \tag{17}$$

In Figure 10, v_r is plotted as a function of C_{dc} for different loading conditions. In this figure, C_{dc} is ranged from 100 μF to 1000 μF and also a fixed value of 70 μsec is considered for τ. According to Figure 10, the dc voltage ripple is in an acceptable range for a wide variety of capacitor sizes and it reaches below 5 percent for C_{dc} higher than 500 μF. The highest ripple is 8.8 percent of V_{C0} for C_{dc} equal to 100 μF under the light load conditions.

Furthermore, C_{dc} can affect the value of V_{C0} according to (13). In Figure 11, V_{C0} is plotted as a function of C_{dc} for the rated machine speed and current. It can be seen from this figure that V_{C0} decreases, but not significantly, as C_{dc} is increased. To sum up, V_{C0} totally decreases as the time duration τ and C_{dc} are increased. On the other hand, the devices current ratings increase as τ is increased. Therefore, a simple compromise must be made in order to have the best dimensioning for the VSI components according to the load conditions. As mentioned previously, the only factor controlled by the VSI switching is the time duration τ. Thus, this value can be treated as a proper constant, e.g. 70 μsec for the machine and load specifications stated in Table I, under different operating conditions.

The ripple factor, v_r , is determined in terms of the voltage variations ΔV_{dc} and V_{C0} as [22]:

$$v_r=\frac{\Delta V_{dc}}{V_{C0}} \tag{18}$$

TABLE I. CHARACTERISTIC DATA OF THE WFSM.

Apparent power	1000 (kVA)	q-axis magnetizing inductance, L_{mq},	0.53 (mH)
Line-to-line voltage	570 (V)	d-axis magnetizing inductance, L_{md},	0.632 (mH)
Line current	1034 (A)	*d-axis damper leakage inductance, L_{lkd},	0.015 (mH)
Frequency	100 (Hz)	*q-axis damper leakage inductance, L_{lkq},	0.024 (mH)
Number of poles	4	*Field leakage inductance, L_{lf},	0.050 (mH)
Stator leakage inductance, L_{ls},	0.07 (mH)	Commutation inductance, L_C,	0.087 (mH)

* Rotor quantities are referred to the stator.

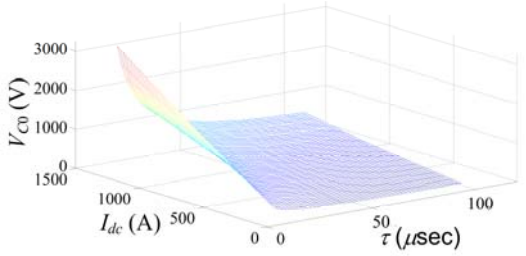

Fig. 8. V_{C0} as a function of τ under different operating conditions (C_{dc}=500 μF).

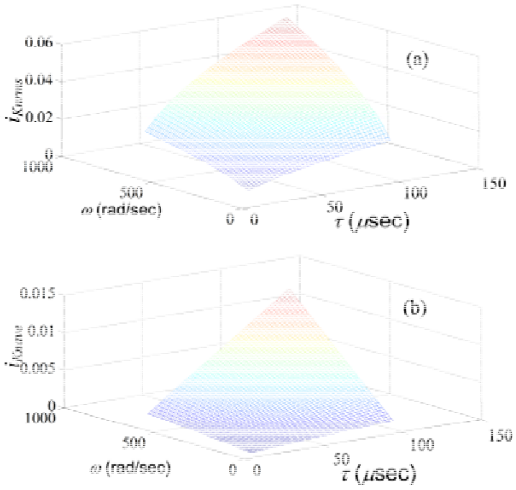

Fig. 9. Current ratings of VSI switches as a function of τ for different motor speeds (C_{dc}= 500 μF) , (a) i_{Knrms} and (b) i_{Knave}.

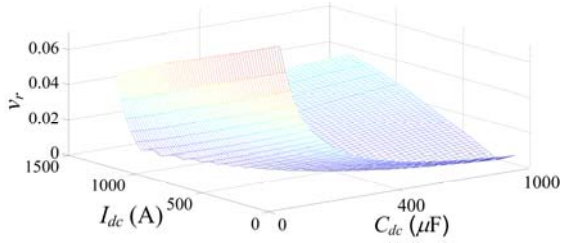

Fig. 10. DC capacitor voltage ripples as a function of C_{dc} (τ=70 μsec).

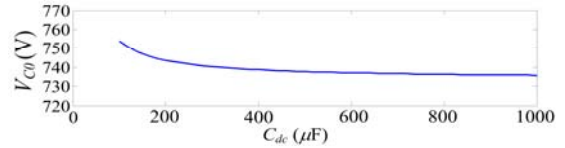

Fig. 11. V_{C0} as a function of C_{dc} (τ=70 μsec) for rated operating condition.

V. SIMULATION RESULTS

In this Section, dynamic model of the WFSM with the specifications highlighted in Table I in rotor *d-q* reference frame is implemented in MATLAB/Simulink software [24] and the proposed five-level CSI is utilized to drive the machine. The results are compared with those of a three-level counterpart. FOC in stator flux reference frame [23] is also used as the drive strategy. In the simulations, C_{dc} and τ are considered equal to 500 μF and 70 μsec, respectively. Also, the dc-link inductance, L_{dc} in Figure 1, is equal to 20 mH. This Section is divided into two subsections. In the first subsection, the results are shown for normal operating conditions and in the second part, the performance of the proposed inverter is studied during starting of the machine which can be an important issue in the case of conventional LCI-fed WFSM drives.

A. Normal Operatind Condition

In Figure 12, machine stator phase '*a*' current and voltage waveforms are shown when the machine is supplied from the proposed converter scheme and running at the speed of 2100 rpm (70 Hz). The firing angle of the thyristors is set to 165°. In the resultant five-level waveform of the current, the phase shift between fundamental components of phase current and voltage, φ in Figure 2, is equal to $\pi-\alpha-\pi/12$. Therefore, unity power factor operation (UPF) for the fundamental components of the stator phase current and voltage is almost achieved that can be also concluded from Figure 12. From Figure 12, two types of distortion are observable in the stator phase voltage: voltage notches which are due to the load commutation in LCI and voltage spikes which are produced during the commutation instants in CSI. The depth and duration of the voltage notches depend upon thyristors firing angle, α in Figure 2, dc-link current, $I_{dc}/2$, commutation inductance, L_C, motor speed, ω, and back EMF. In addition to these parameters, voltage spikes are also affected by the time duration τ. As τ increases the current variation rate and, consequently, the voltage spikes are decreased at the cost of increased VSI rating.

DC capacitor voltage, v_{cap}, is shown in Figure 13. It is evident from the figure that ripple factor, v_r, is limited to less than 3 percent by using a capacitance of 500 μF. On the other hand, the drive system is simulated under the same conditions, i.e. same motor speed and load torque, in which WFSM is being fed from the conventional three-phase LCI. The motor phase current and voltage waveforms are shown in Figure 14; where, the maximum allowable firing angle, α, for the thyristors is equal to 157° for safe commutation. This means that φ_{LCI} (Figure 2) is equal to 23° which is much higher than φ (Figure 2) equal to zero in the case of five-level converter. Thus, one can expect lower field current and, consequently, lower field losses in the proposed drive. This fact is shown in Figure 15 where the field current waveforms for both converters are compared.

Furthermore, fast Fourier transform (FFT) analysis of the current waveforms shows that the current THD is remarkably decreased for five-level converter. In Table II, the amplitude of the current dominant harmonic components is normalized to the amplitude of the fundamental component for both five-level (Figure 12) and three-level (Figure 14) current waveforms. According to Table II, the fifth and seventh harmonic components are reduced significantly for the proposed converter. These harmonic components are mostly responsible for the machine large electromagnetic torque pulsations featuring six times the operating frequency. In Figure 16, machine electromagnetic torque is depicted for both five-level

and three-level stator current waveforms. This figure indicates that lower level of current harmonic distortion yields in lower torque pulsations in the case of proposed drive.

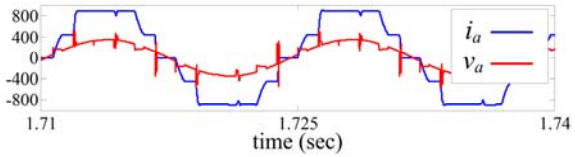

Fig. 12. Stator phase '*a*' current and voltage waveforms when the machine is supplied from the five-level current-source inverter (ω=2100 rpm, I_{dc}/2=445 A, C_{dc}=500 μF and τ=70 μsec).

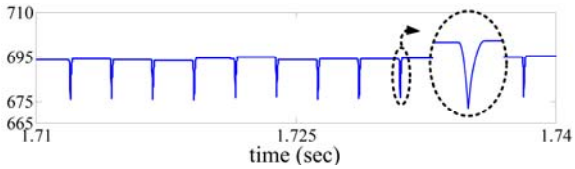

Fig. 13. v_{cap} in the proposed five-level current-source inverter (ω=2100 rpm, I_{dc}/2=445 A, C_{dc}=500 μF and τ=70 μsec).

B. Start-up

DC-link pulsing method is widely used in industrial LCI-fed WFSM drives such as gas turbine starters [7] to control the machine during starting as well as at low-speed operation (≤10%). However this method generates pulsating current and torque with a reduced average torque. On the contrary, the proposed converter is also beneficial in start-up and at low-speed operation of the machine. For these conditions, the firing pulses are not released for thyristors in LCI and the CSI and voltage clamping VSI (Figure 1) are switched according to the procedure explained in subsection III.*B*. Consequently a three-level current waveform is available for the stator phase currents. In Figure 17, simulation result for the stator phase current is shown when the machine is fed from the CSI and running at the speed of 90 rpm (0.03 pu). For comparison, Figure 18 shows the simulation result in which the machine is supplied from LCI and dc-link pulsing method is utilized for the same loading conditions. The interruptions in the stator phase current are due to the zero intervals in the dc-link current which must be applied every sixty electrical degrees, because the commutation are taken place every one-sixth of the period (see Figure 3). These interruptions reduce the active power for the same dc-link current, I_{dc}, comparing to the case in which the machine is fed from the CSI. Thus, the output of the speed controller, I_{dcref}, will be higher in the dc-link pulsing method for the same load torque. Also, the interruptions produce notches in the electromagnetic torque which can be detrimental for mechanical parts specifically for the drives with intermittent startings. In Figure 19, the resultant torque waveforms are shown for both cases. A much smoother torque for low-speed operation is observable from the proposed drive scheme.

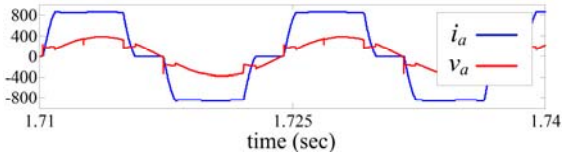

Fig. 14. Stator phase '*a*' current and voltage waveforms when the machine is supplied from the conventional three-level LCI (ω=2100 rpm, I_{dc}=850 A).

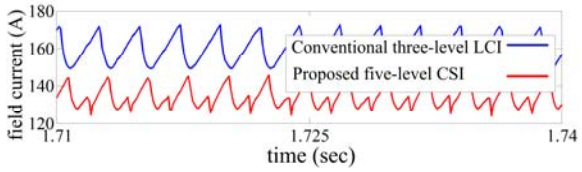

Fig. 15. Field current of WFSM (ω=2100 rpm).

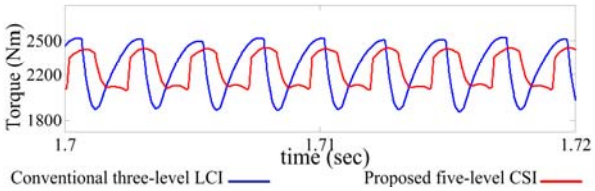

Fig. 16. Electromagnetic torque of WFSM (ω=2100 rpm).

TABLE II. PHASE CURRENT FUNDAMENTAL, I_{af}, AND HARMONIC COMPONENTS AS A PERCENTAGE OF I_{af} FOR THE PROPOSED CSI AND CONVENTIONAL LCI (ω=2100 RPM).

	I_{af} (A)	I_{a5} (%)	I_{a7} (%)	I_{a11} (%)	I_{a13} (%)	THD (%)
Five-level CSI	953	8.35	0.34	6.97	6.12	14.11
Conventional LCI	931	18.22	11.88	5.57	3.81	23

VI. DISCUSSIONS AND COMPARISON WITH OTHER MULTILEVEL CSI STRUCTURES

So far, several multilevel CSI configurations are presented in literature for motor drive applications, most of them utilizing PWM techniques as their switching strategy. On the other hand, to the best of authors' knowledge, there is only [25] that has focused on the multilevel CSI-fed induction motor drive in which the power electronic devices are switched at the machine working frequency. In [25], a multilevel current waveform is obtained for the machine stator current by adding the output currents of one LCI and one CSI. A three-phase capacitor bank is considered at the machine terminals to generate the leading power factor for the natural commutation of the LCI switches. On the other hand, in order to minimize the size of the capacitor bank a phase-shift of 60 degrees is computed to be considered between the LCI and CSI output currents. With this phase-shift, a four-level current waveform is obtained with a THD of approximately 24% (see Figure 2b) while it is around 10% in the proposed five-level CSI (it should be mentioned that in Figure 2b only the 5th and the 7th harmonic components

are taken into account and the dc-link current is assumed to be smooth).

Despite several advantages of the proposed multilevel CSI configuration in the WFSM drive system, there are few limitations regarding the VSI switches. Although the current rating of the VSI switches is much lower than that of the CSI and the LCI switches, the VSI devices conduct the dc-link current during the commutation periods of CSI. Thus, attention is required to select the devices which can tolerate surge currents equal to the dc-link current value at rated operating conditions.

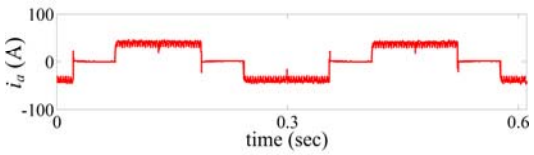

Fig. 17. Stator phase current when the machine is supplied from CSI and LCI is turned off during start-up or low-speed operating conditions (f = 3 Hz, I_{dcref}=38 A, C_{dc}=500 μF, τ=70 μsec).

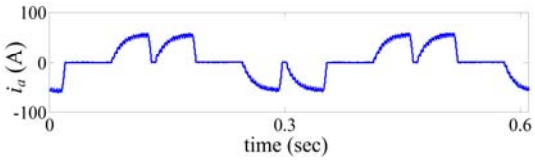

Fig. 18. Stator phase current when the machine is supplied LCI and dc-link pulsing method is applied (f = 3Hz, I_{dcref}=48).

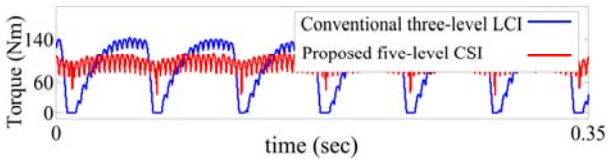

Fig. 19. Machine electromagnetic torque (f = 3Hz).

VII. CONCLUSION

This paper proposes to add a CSI, which is switched at machine operating frequency, to the conventional three-phase LCI's to improve the characteristics and performance of the high-power LCI-fed WFSM drives. To avoid large voltage spikes at the commutation instants, a voltage clamping circuit is used. Accordingly, a five-level waveform for the output current is acquired. Lower harmonic distortion of the output current results in lower torque pulsations and lower harmonic losses of the windings comparing with the conventional LCI's. Also, the air-gap flux will be less distorted which yields in lower iron losses. Furthermore, unity power factor operation is achieved for a wide range of machine speed, thus, decreasing the field current and its consequent losses. Moreover, torque notches produced by the dc-link pulsing method at start-up and at low speeds are removed by the introduced converter.

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