Cyclic bend tests for the reliability evaluation of printed circuit boards under dynamic loads

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ABSTRACT. The reliability of printed circuit boards under dynamic loads is a key issue in the handheld electronic products industry. In order to predict the performance of the boards in their application lifetime, different tests were developed. The current industry-wide standard testing method is a board level drop test. In this test, the boards are dropped under defined conditions until a failure in the board is detected. The main failure driver is a flexural oscillation of the board due to the impact event. As this test method has a number of drawbacks, an alternative test method was evaluated in this study. A board level cyclic bend test was used and the results of both tests were compared. A very good correlation between the methods could be observed, supporting the suitability of the board level cyclic bend test for the determination of the drop test performance. The advantages of the alternative test method were shorter testing times, better adaptability and test simulations at lower computing time. In future analysis, test simulations will be used to generate Wöhler curves related to the local stresses.

KEYWORDS. Printed Circuit Board; Reliability; Drop Test; Cyclic Bend Test; Fatigue.

INTRODUCTION

The performance of printed circuit boards (PCBs) under dynamic loads is of significant interest due to the increasing market for handheld electronic products. Because of their size and application, handheld electronic products are especially prone to be dropped, i.e. exposed to an impact load during their useful service life. These impact loads can result in serious damage of the PCB interconnections and thus in the malfunction of the product. To evaluate the drop performance and to develop reliable designs, different board level test methods were introduced. Wong et al. reviewed the development of the methods in their work [1]. A standardized board level drop test (BLDT) JESD22-B111 was defined under the Joint Electronic Device Engineering Council (JEDEC) [2]. In this test defined drops of the PCBs are repeated until failure is detected. The rather complex test set-up and load application affect the test robustness. Drawbacks of the standardized BLDT are discussed in literature e.g. by Wong et. al [1, 3] and Luan et. al [4]. Apart from the poor reproducibility, the main criticisms are the slow test throughput and the lack of relevance to the product drop impact performance.
Thus, in this work an alternative test to determine the drop performance was performed and evaluated. Flexing of the circuit board, due to input acceleration created from dropping, is the primary driver for PCB failure. Therefore, a board level cyclic bend test (BLCBT), applying a repeated and well defined flexure, was used to reproduce the loading situation.

The simplified and accelerated load application should result in a more robust test method, providing faster and more reliable results.
In this study, conventional BLDT and BLCBT were performed for a set of PCBs. The results were compared to evaluate the suitability of cyclic bend tests as an alternative test method.
The test method applied was based on similar ideas to the high speed cyclic bend test (HSCBT) [5, 6], but was realized under different loading conditions. The specimens were loaded under three-point bending and significantly higher deflection amplitudes were used.

MATERIALS AND SPECIMENS

PCBs with different layer build-ups, expected to differ significantly regarding their BLDT performance, were tested. The aim was to simplify the comparison of the testing methods by covering a wide range of BLDT performances.
The analyzed specimens were eight layer PCBs and six different layer build-ups were tested. These build-ups differed regarding the intermediate epoxy layers which are glass-fibre reinforced in most cases. Only for the surface layers it can in some cases be advantageous to use neat epoxy resin. Thus, variations in the reinforcement of the surface layers were considered in the test plan. Additionally, different epoxy resin types were analyzed. A detailed summary of the materials used in the different layers (Core, IL1, IL2 and IL3) of the tested PCB designs is provided in Tab. 1. The abbreviations M1, M2, M3 and M4 represent different manufactures and epoxy resin types respectively, PP indicates a Prepreg layer (glass fibre reinforced) and R stands for an unreinforced and neat epoxy resin layer. PP1 and PP2 differ regarding the glass fibre mat used for reinforcement. The layers marked with b are the low dielectric constant versions of the layers marked with a. A schematic representation of the layer assignments in the build-up, including the epoxy layer thicknesses, is shown in Fig. 1. All copper layers had a thickness of 18 µm.

Design Nr.	Core	IL1	IL2	IL3
	Material			
1	*M1 a*	*M1 PP 1a*	*M1 PP 2a*	*M3* R
2	*M1 a*	*M1 PP 1a*	*M1 PP 2a*	*M1 PP 2a*
3	*M1 a*	*M1 PP 1a*	*M1 PP 2a*	*M4* R
4	*M2*	*M2 PP1*	*M2 PP2*	*M3* R
5	*M2*	*M2 PP1*	*M2 PP2*	*M2 PP2*
6	*M1 b*	*M1 PP1 b*	*M1 PP2 b*	*M3* R

Table 1: An overview of the chosen materials for the specified layers in the six PCB designs tested.

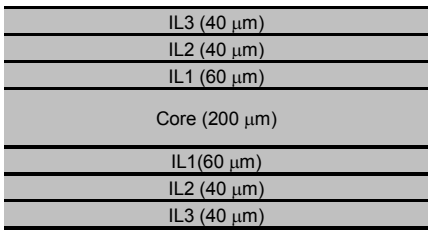


Figure 1: A schematic representation of the layer assignments in the PCB build-up.

The PCB geometry was chosen following the JEDEC standard, but was adapted according to customer requirements. The defined board geometry is shown in Fig. 2. The darker squares at the board centre represent the mounted components. Only two components instead of 15 were used to simplify the test. The two most failure-prone components, with regard to the PCB manufactures experience, were chosen. The components were daisy chained according to the standards.

BOARD LEVEL DROP TEST ANALYSIS

Before the development of an alternative test method, it was necessary to analyze the acting loads and resulting PCB deformation in a standard BLDT. The drawn conclusions should help designing a reasonable test.
Except for some adapted parameters, the analyzed BLDT was performed according to the JEDEC standard. An

alternative board geometry, described in *Materials and specimens* chapter, and a different board fixation (longer standoffs) were used. The drop height and strike surface were adjusted to achieve a specified G level of 1500 g peak acceleration and a pulse duration of 1 ms.
Drops were repeated until first failure was detected. Failure was defined as an electrical discontinuity in the daisy chains of resistance greater than 1000 ohms lasting for 1 microsecond or longer. To measure the very short lasting electrical discontinuities a special event detector (256STD, Analysis Tech, Wakefield, US) was used.
For the BLDT analysis a high-speed camera (Fastcam SA1.1, Photron Inc., San Diego, US) was used. In Fig. 3 the BLDT set-up is shown. The board is fixed with four screws at its corners on the drop table. The test, i.e. the impact of the drop table on the strike surface was filmed with the high-speed camera.

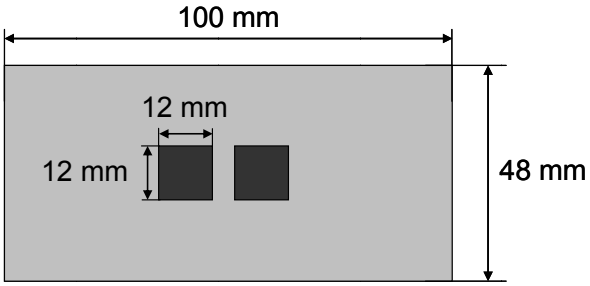


Figure 2: A schematic presentation of the used PCB geometry. The darker squares represent the mounted components.

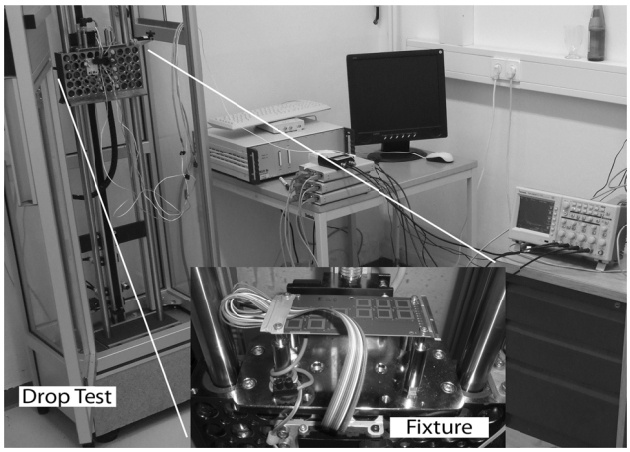


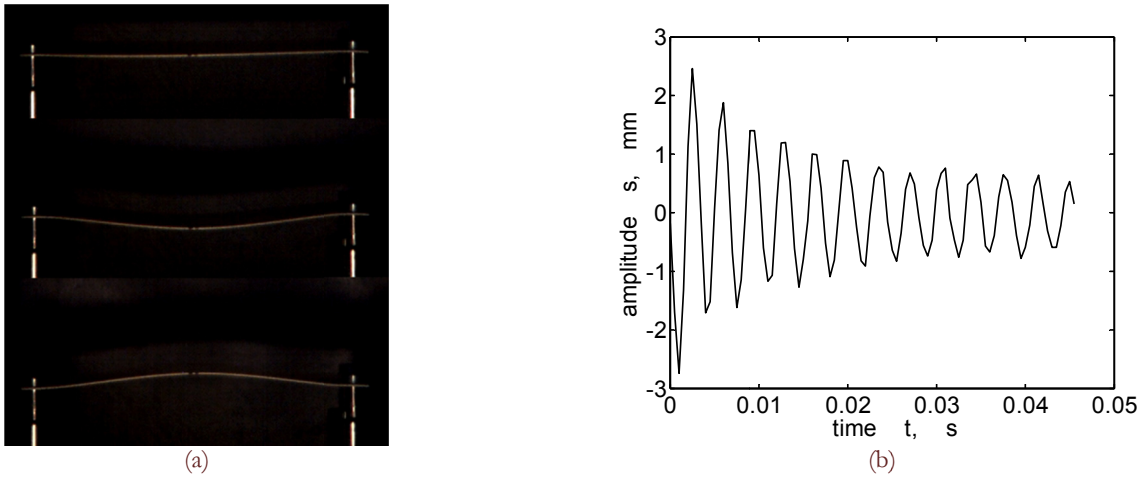
Figure 3: The test set-up of the JESD22-B111 board level drop test.

In Fig. 4a), starting from the top, three consecutive high-speed camera images show the impact of the PCB. The board is set in a damped bending-oscillation, which can be recorded by a camera. Using image analysis software (Viana 3.64, Thomas Kersting, Institute for Didactics and Physics, University of Essen, DE), an oscillogram of the PCB centre deflection could be generated (Fig. 4b). The initial oscillation frequency was determined as 280 Hz.
Furthermore, strain gauges were placed at the PCB surface centre to measure the maximum occurring longitudinal strains. The observed longitudinal strain values at the first deflection were 2×10^{-3}.
From the analysis results it could be concluded that the main deformation mechanism and consequently failure driver is the bending-oscillation. Knowing this, it seemed reasonable to expect correlating results from a BLCBT, where a sinusoidal cyclic bending load is applied.

BOARD LEVEL CYCLIC BEND TEST DEVELOPMENT

For the load generation an electro-dynamic testing machine (Bose ElectroForce 3450, Bose Corporation, Eden Prairie, US) was used. This machine has the advantage of a very precise force and displacement control and was used to apply a sinusoidal displacement amplitude.

For the board fixation a three-point bending fixture was constructed, where the board is placed centred on support rollers (Ø 5 mm) which have a distance of 90 mm to each other. The load is applied by a fin, which consists of two rollers (Ø 5 mm), clamping the board at half length. The clamping force was applied over spring plungers to have a defined load. A schematic representation of the fixation is shown in Fig. 5.



(a) (b)

Figure 4: The results of the JESD22-B111 board level drop test high-speed camera analysis. In a) chosen consecutive high-speed camera pictures show the development of the PCB deflection right after the impact. In b) the according amplitude oscilloagram is presented.

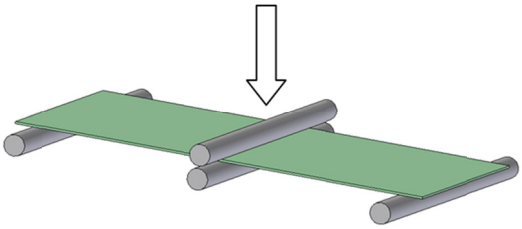


Figure 5: A schematic representation of the three-point bending fixture used in the board level cyclic bend test.

It needs to be considered that the board is not clamped at the position of the support rollers, implicating that the load can only be applied in one direction. A set-up with clamps at the support rollers would have resulted in an overconstrained system. Robustness and reproducibility of the test would have been affected, counteracting previous efforts. Therefore, it was accepted that in contrast to the actual BLDT alternating loads could not be applied.

The test parameters were derived from the BLDT analysis. The maximum peak-to-peak oscillation amplitude in the BLDT was about 5 mm and the maximum fibre strain was about 2 x 10^{-3}. For the BLCBT peak-to-peak amplitudes of 4mm with a mean deflection of 3mm (BLCBT Set-Up 1) and 3mm with a mean deflection of 2.5mm (BLCBT Set-Up 2) were chosen. The maximum fibre strains were 1.7 x 10^{-3} and 2.2 x 10^{-3}, that is in the range of the BLDT. The minimum deflection of -1mm was defined to ensure that no lift-off of the board from the support rollers could occur in the tests.

Due to machine limits, it was not possible to perform the tests at the oscillation frequency of the impacted PCB in the BLDT (280 Hz). To remain at the desired optimum machine displacement control precision the frequency was kept at 25 Hz.

A picture of the final test set-up is shown in Fig. 6. The event detector was used in the same way as for the BLDT.

EXPERIMENTAL METHOD COMPARISON

The BLDT was performed with nine samples of every PCB build-up to obtain representative results and to apply statistics. For the BLCBT, as indicated in *Board level cyclic bend test development* chapter, two different set-ups were used. Three boards for all designs and both set-ups were tested to decide which performs better. For the chosen set-up another five test repetitions were planned to apply statistics according to the BLDT evaluation.

For the BLDT, the number of drops until the first failure, detected by the event detector, was taken as evaluation parameter. Analogous, for the BLCBT the number of cycles until failure was measured.

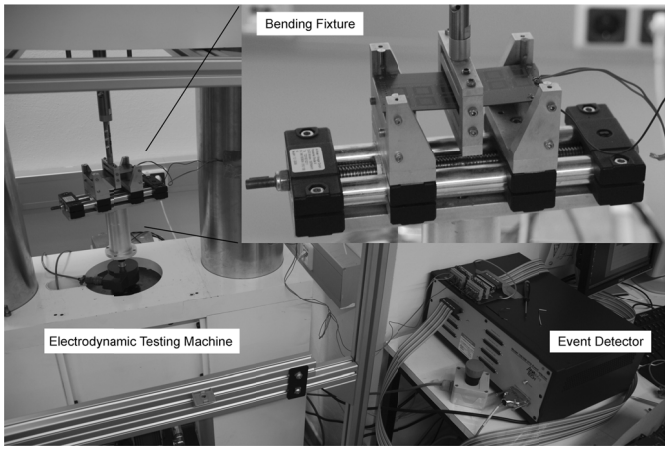


Figure 6: The test set-up of the board level cyclic bend test.

To compare the BLDT with the BLCBT the method average results for the different PCB build-ups were plotted against each other and a Pearson's r factor [7] was calculated to rate the linear correlation. A schematic representation of the method comparison is shown in Fig. 7.

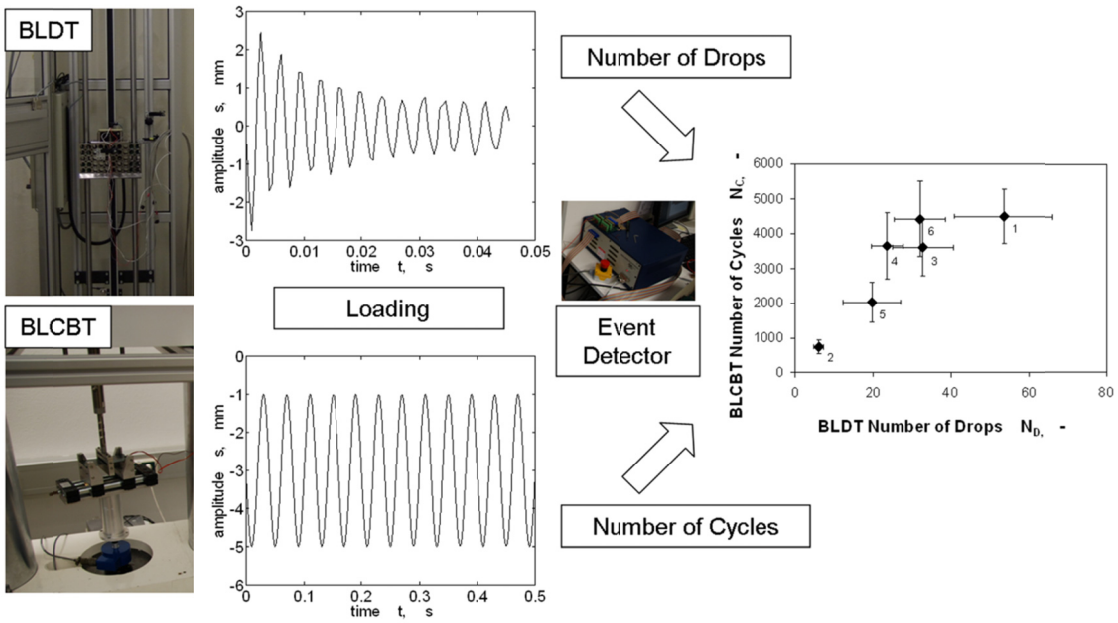


Figure 7: Schematic representation of the comparison of BLDT and BLCBT.

Furthermore, to check the correlation of the failures types introduced by the different testing methods, a failure pattern analysis was performed. Microsections of the expected failure locations were prepared and analyzed with a light microscope. It was tested if the same failure modes occur despite the different loading conditions.
Finally, as it is advantageous to use the Weibull distribution in reliability and life data analysis, similar to the BLDT analysis (e.g. [8, 9]), Weibull-parameters were determined to allow for a comparison of the methods on the basis of a statistical evaluation.
Therefore, a fictitious time-to-failure had to be calculated for all BLDT results to have a correlating parameter to the time-to-failure in the BLCBT. A conversion factor was introduced by dividing the average time-to-failure of all build-ups in the

BLCBT through the average number of drops of all PCB build-ups in the BLDT. This factor was used to calculate fictitious times-to-failure based on the number of drops until failure of the BLDT.

RESULTS AND DISCUSSION

The results of the performed BLDT are presented in Fig. 8 in terms of drops until failure. The pillars represent the average of nine measurements respectively. The results show the desired wide range of board BLDT performances for the six tested build-ups. The large gap between designs 1 and 2 results from the influence of the reinforcement in the surface layers. While design 1, having unreinforced outer layers (IL3), performed very well, design 2, built with glass fibre reinforced IL3 layers, performed worst of all designs. In design 3 a different neat epoxy resin type was used for the IL3 layers, resulting in a worse BLDT performance compared to design 1. For designs 4 and 5 the same effect, regarding the reinforcement of the IL3 layers, could be observed as for designs 1 and 2. The effect was less pronounced, apparently due to the different material manufactures. Design 6 was a low dielectric constant epoxy resin version of design 1, resulting in a BLDT performance in the range of design 3.

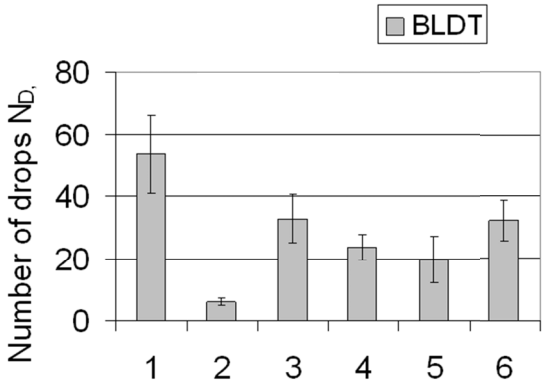


Figure 8: Results of the BLDT performed on six PCB designs. Additional to the average values the standard deviations are indicated.

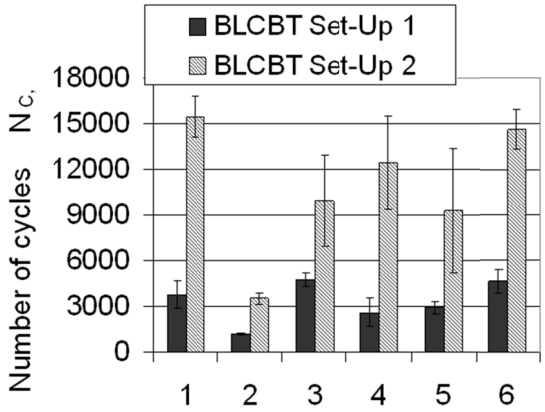


Figure 9: BLCBT results showing the amplitude dependence. Additional to the average values the standard deviations are indicated.

BLCBT with two different set-ups were performed on three specimens for every design. The average results of BLCBT Set-Up 1 and BLCBT Set-Up 2 are presented in Fig. 9 in terms of cycles until failure. As expected, set-up 2, with the application of the lower deflection amplitude, resulted in significant longer times until failure. Nevertheless, if expressed in percentage, the differences between the tested designs were very similar for the set-ups. As set-up 2 did not have an advantage regarding the measurement scatter, the faster set-up 1 was chosen for further tests.
Five more specimens were tested with set-up 1 to be able to perform a statistic evaluation of the data. In Fig. 10 the BLDT results were compared with the BLCBT results of set-up 1. The number of cycles until failure in the BLCBT was

plotted over the number of drops until failure in the BLDT. The plot is revealing a clear method correlation and the Pearson's r factor, determined as 0.87, supported the method hypothesis. However, because of existing discrepancies from the linear correlation, which can be attributed to the existing data scatter on the one hand and on the unregarded loading condition dependent material behaviour on the other hand, only significant differences in the BLDT behaviour can be expected to be reflected in the BLCBT.

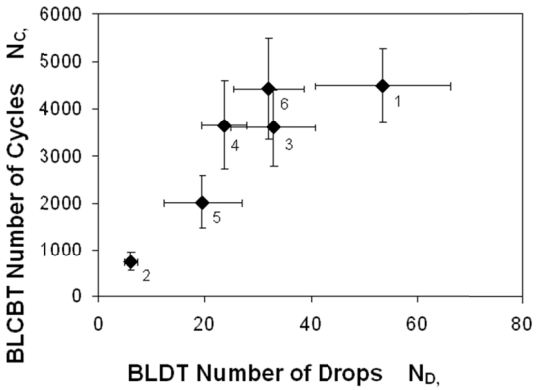
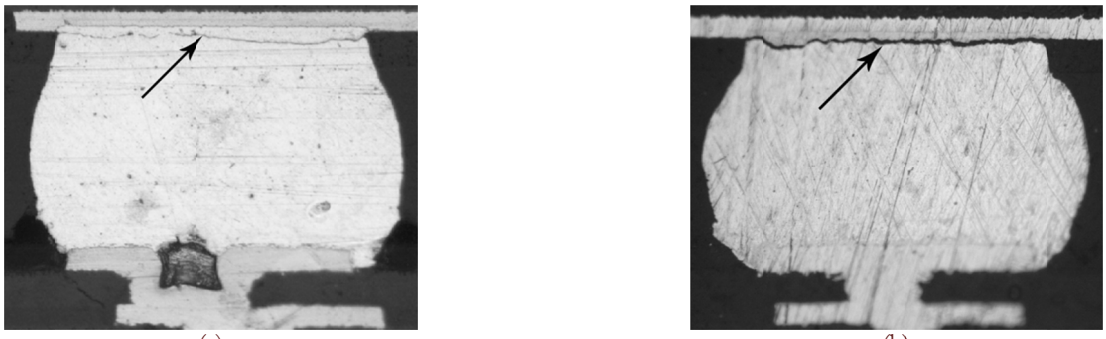
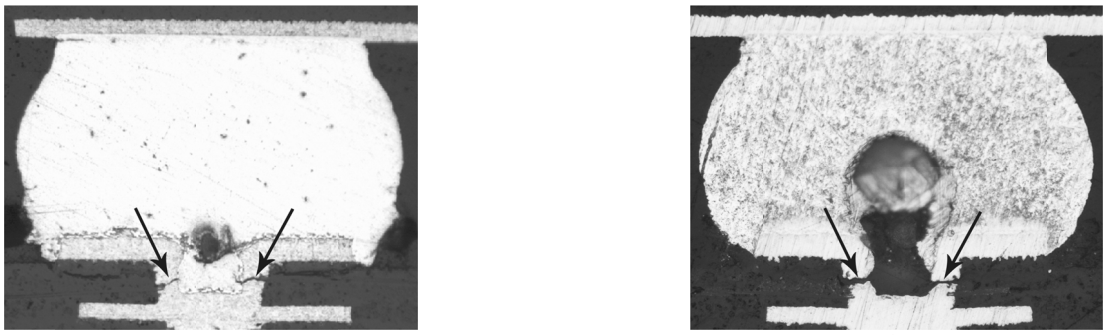


Figure 10: Comparison of the BLDT and BLCBT set-up 1 results for six PCB designs. Additional to the average values the standard deviations are indicated.



(a) (b)

Figure 11: Comparison of a) the failure of design 1 in the BLDT and b) the failure of design 1 in the BLCBT, analyzed with light microscopy.



(a) (b)

Figure 12: Comparison of a) the failure of design 2 in the BLDT and b) the failure of design 2 in the BLCBT, analyzed with light microscopy.

Moreover, to verify the accordance between BLCBT and BLDT a failure pattern analysis was performed on the tested specimens. The analysis was focused on designs 1 and 2, expected to exhibit the most pronounced differences in the failure mode. In Fig. 11 and Fig. 12 the light microscopy images of identified failure locations are shown. The cross

sectional areas of the two-sided cut sphere represent the solder ball connecting the printed circuit board (at the bottom of the image) with the mounted component (at the top of the image). The detected failures are indicated by black arrows. The failures correspond to typical failure patterns mentioned in literature e.g. [4, 9-12]. In Fig. 11 the failure of design 1 in the BLDT (Fig. 11a) is compared to the failure of design 1 in the BLCBT (Fig. 11 b). A matching failure location could be observed. The solder ball was cracked close to the mounted components. In Fig. 12 the failure of design 2 in the BLDT (Fig. 12 a) is compared to the failure of design 2 in the BLCBT (Fig. 12b). Again, the failure location was the same for both test methods, but different from the design 1 location. Failure occurred in the copper interconnections in the board and not in the solder ball. Thus, it could be shown that both methods led to the same failure modes for the examined design 1 and 2, which further supports the correlation of the methods.
A statistical comparison of the BLDT and BLCBT results was based on the Weibull distribution [13].

$$y = abx^{b-1}e^{-ax^b} \tag{1}$$

The parameters a, the scale parameter, and b, the shape parameter, are given for all analyzed designs in Tab. 2. The times to failure of the BLDT are fictive values and were calculated as described in *Experimental method comparison* chapter. The performance trend in the BLDT Weibull analysis is matched to the performance trend in the BLCBT Weibull analysis for all examined designs. In Fig. 13 the difference between the Weibull distribution for designs 1 and 2 is shown graphically.

PCB Design	1		2		3		4		5		6	
Weibull Parameter	a	b	a	b	a	b	a	b	a	b	a	b
BLDT	*240.4*	*2.4*	*27.4*	*2.7*	*147.4*	*2.4*	*104.8*	*3.6*	*86.6*	*1.5*	*143.3*	*2.8*
BLCBT	*200.4*	*3.7*	*33.9*	*2.1*	*159.2*	*2.4*	*165.6*	*2.3*	*90.0*	*1.9*	*197.3*	*2.3*

Table 2: Two-parameter Weibull distributions for all tested PCB designs are compared for the BLDT and the BLCBT.

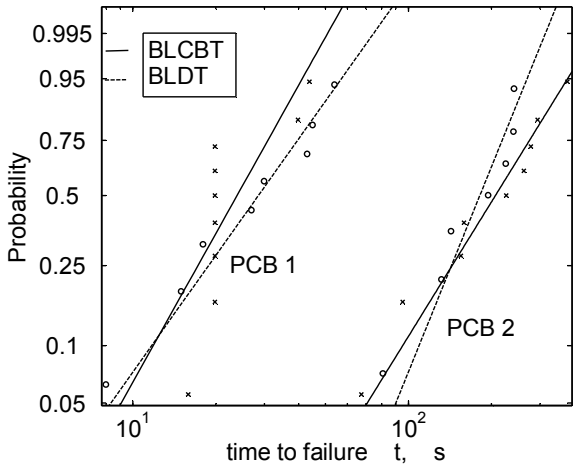


Figure 13: The graphical representation of the two-parameter Weibull distributions for designs 1 and 2. The results of both methods, the BLDT and the BLCBT are presented.

SUMMARY AND CONCLUSION

The JESD22-B111 board level drop test (BLDT) is the current state of the art to evaluate the reliability and lifetime of PCBs under impact loads. As the rather complex test set-up implicates some drawbacks such as poor reproducibility and slow test throughputs, an alternative test method was analyzed. A board level cyclic bend test (BLCBT) was evaluated. In this method, instead of repeated drops, a controlled cyclic displacement is applied on the PCBs.
The two methods were compared and evaluated for six different PCB designs. The results correlated very well and therefore the BLCBT may be used to estimate the BLDT performance. This conclusion was supported by a performed failure analysis showing that the design dependent failure modes were independent of the test method. Additionally, a

statistical evaluation based on a two-parameter Weibull distribution was performed. The statistical results supported the good approach of the two methods.
Finally, the following advantages of the BLCBT over the BLDT could be identified:

- ✓ The BLCBT testing time is significantly shorter than the BLDT testing time (The factor between the method testing times depends on the board performances. The better a board performs, the faster is the BLCBT compared to the BLDT. In our case the BLCBT was about two times faster than the BLDT. The reason for the testing time differences is an approximate break of 5 seconds between each drop in the BLDT.)
- ✓ The BLCBT can be performed considering different influence parameters (e.g. temperature, frequency or amplitude) by default. In contrast the BLDT under temperature influence is costly, as the temperature has to be applied on a large testing space. Furthermore, in the BLDT only the initial amplitude can be controlled. As this is done by adapting the impact energy, an adjustment to predefined amplitudes is difficult. The frequency in BLDT can hardly be varied at all.
- ✓ The BLCBT can be performed on basically every dynamic testing machine which is capable of applying the desired displacement and frequency.
- ✓ The BLCBT can be simulated at lower computing times than the BLDT using the Finite Element Method. Simulations of the BLDT are difficult, as the load application and the definition of the boundary conditions are challenging [14, 16]. The simplest way to simulate the BLDT is the 'Input-G method' [13, 17, 18, 20, 21]), where an acceleration signal is applied directly to the board, which is still computationally expensive.

In future analysis it is planned to generate Wöhler curves [22] to evaluate the fatigue behaviour of PCB designs. Therefore, BLCBT will be performed at different deflection levels. To determine the acting local stresses, finite element simulations are planned.
Thus, having the local failure stresses in dependence of the PCB bending amplitudes, it would be possible to plot the local failure stress over the number of cycles. This resulting Wöhler curves should help to improve the understanding and the prediction of the PCB fatigue behaviour.

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