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IMPACT OF CHANNEL ENGINEERING ($SI_{1-0.25}GE_{0.25}$) TECHNIQUE ON G_M (TRANSCONDUCTANCE) AND ITS HIGHER ORDER DERIVATIVES OF 3D CONVENTIONAL AND WAVY JUNCTIONLESS FINFETS (JLT)

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Abstract. *The paper explores the analog analysis and higher order derivatives of drain current (I_D) at gate source voltage (V_{GS}), by introducing channel engineering technique of 3D conventional and Wavy Junctionless FinFETs (JLT) as silicon germanium ($Si_{1-0.25}Ge_{0.25}$) device layer. In view of this, the performances are carried out for different gate length (L_G) values (15-30 nm) and current characteristics determined by maintaining constant ON current (I_{ON} 10^{-5}) (A/μm) for both devices. With respect to this, a comparison has been made between these MOS structures at molefraction x = 0.25 and it was found that the electric field is perpendicular to the current flow which induces volume inversion approach. Accordingly, for the simulation study better channel controllability over the gate is observed for Wavy structures and high I_D induces as the L_G scales down. With respect to this the constant I_{ON} determine I_D, transconductance (g_m), transconductance generation factor (TGF) and its higher order terms ($g^{\backslash}_m$, and $g^{\backslash\backslash}_m$) of the devices are studied with relaxed SiGe approximation. The extensive simulation study on short channel (SC) parameters are also performed and it is observed that the Wavy JL FinFET shows less sensitivity towards short channel effects (SCEs) over conventional one, therefore the dependency of N-type doping concentration (N_D = $1.7x10^{19}$ cm^{-3}) and metal workfunction (ϕ_M = 4.6 eV) are responsible to achieving reduced SCEs.*

Key words: *SiGe JL FinFET, channel engineering, molefraction, analog parameters, higher order derivatives, short channel parameters (SC).*

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1. INTRODUCTION

Due to the tremendous growth in technology, the exploration of novel architectures has become mandatory for ultra large scale integration (ULSI) applications. Among various architectures, the FinFET has become an attractive device solution for down scaling the SCEs. As the device dimensions have moved to nanometer range [1]–[4], this primarily owes to its superior gate control over channel. Multi-gate structures like Silicon on insulator (SOI) MOSFETS [5], [6] are scaled down to decananometer range, however realizing these MOSFETS in decananometer [7] range requires extremely sharp source/drain p-n regions which are possibly achieved through high end annealing techniques and there by increases the fabrication cost. To overcome these difficulties a new MOSFET without source/drain p-n junction was proposed [8], [9], and named junctionless nanowire transistor. The comparative study was performed between fabricated Junctionless FinFET (JLT) and conventional bulk FinFET, realizing the SCEs as discussed in [10]. Heavily doped JLT induces fully depleted channel in the subthreshold region with high vertical electric field (E-field). The E-field is neutral at the inversion mode of operation and the shift in V_{TH} occurs when the bands ($\phi_M - \phi_S$) are flat at flat band voltage (V_{FB}) [9]. The absence of doping concentration gradients eliminates diffusion impurities and the sharp doping profile problem. The paper explores the multi-gate JL FinFET topology which is an extended work of [11], [12], this mainly concentrating the analog performances and the higher order g_m parameters using I_D characteristics.

The probabilistic analyses of higher order derivatives are also important to study at scaled L_G, the major issues that emphasize the analog and higher order derivatives are important for advance communication system. Non-linearity characteristics realizes unwanted disturbances with frequencies differences at input once, which generates Intermodulation Distortion (IMD) at output stage [13]–[15].

The higher order analysis and the inter-modulation harmonics are important to maintain minimal linearity's at the RF stage [16]. Accordingly, at pre-fabrication process the analog performance parameters are necessary at nanoscale regime. The paper discusses the higher order derivative parameters of 3D conventional and Wavy JL FinFETs using channel engineering scheme. Along with the introduction, Section 2 discusses the device architecture specifications and the simulation procedure undertaken, Section 3 includes the comparative analysis on analog performances of these devices using $Si_{1-0.25}Ge_{0.25}$ material as device layer. Finally, the conclusion is drawn.

2. DEVICE DESCRIPTION AND SIMULATION FRAMEWORK

The multi-gate transistors are the basic step to scale down the SCEs, the challenges and the issues are discussed in [17] and their performance metrics is given in [18]. A thin dual gate approach on SOI with the volume inversion is reported in [5], [19]. The another representation using 2D planar UTB and 3D non-planar approach is first given by [20], [21] later provides the detailed analysis with several performance metrics analyzed and reported in [22]–[24]. The significance of the FinFET provides better layout area efficiency in the digital circuits [25]. In general, the Fin utilizes the availability of single Fin per pitch, in which most of the pitch area is unused. To overcome this, the FinFET limits the current per pitch technology representation. Therefore, the pitch area in FinFET utilizes fully

depleted SOI (FD-SOI) topology which is grown epitaxial and merged with the 2D-FinFET forming a single device with common gate [21]. Utilizing these two approaches, a comparative analog analysis has been performed using channel engineering technique (SiGe material) with the Junctionless FinFET topology. In this section the architectural representation of conventional JL devices and Wavy-JLT is shown in Fig. 1(a), (b). Accordingly, the parameters required to construct the devices are tabulated in Table 1. The structural design is observed for different L_G for 15-30 nm with a uniform doping concentration N_D = 1.7 x10^{19} cm^{-3}, and using high-k (HfO_2) gate side wall spacer's.

The simulations are carried out using sentaurus TCAD [26] simulator. Phillips Unified Mobility Model is used with Lombardi model to account for high-κ induced carrier mobility degradation as considered [27]. For a deeper understanding of the quantum confinement effect, the thickness of Fin and UTB determine the density gradient based quantization models that are used. Inversion Accumulation layer Mobility model includes doping and transverse field dependency, which in turn accounts for a Coulomb impurity scattering being used.

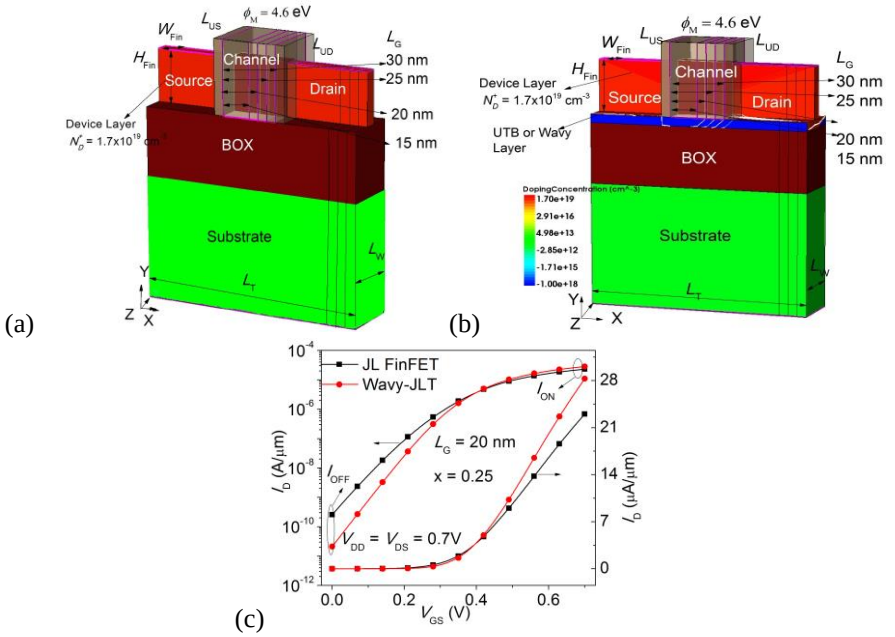

Fig. 1 A 3D representation of (a) Conventional JL FinFET, (b) Wavy-JL FinFET at L_G = 15-30 nm (c) I_D-V_{GS} characteristics of Conventional and Wavy JL FinFET at L_G = 20 nm and x = 0.25.

To account for the longitudinal and vertical electron field an effective intrinsic density, OldSlotboom band gap narrowing model [28], Shockley-Read-Hall mechanism for generation and recombination [29], and quantum mechanical effects are included. The device physical properties are discretized onto a non-uniform mesh of nodes and simulated with appropriate parameterization models [30]. The same models are considered for the

simulation study to observe the performance of the devices. With respective to this, the I_D-V_{GS} characteristics are plotted and shown in Fig. 1(c) and the I_{ON} ranges constant for both the device, but a small improvement in I_D is observe for 3D Wavy-JLT.

Table 1 Parameter required for simulation.

Parameters	3D JL FinFET	3D Wavy-JL FinFET
SiGe device layer (W_{Fin})	7 nm	7 nm
SiGe device layer (H_{Fin})	30 nm	30 nm
Silicon thickness (T_{Si})	---------	10 nm
Donor doping (N_D)	1.7x10^{19} cm^{-3}	1.7x10^{19} cm^{-3}
EOT of gate dielectric (T_{OX})	1 nm	1 nm
Gate work Function (ϕ_M)	4.6 eV	4.6 eV
Drain Supply Voltage (V_{DD})	0.05 V, 0.7 V	0.05 V, 0.7 V
Channel length (L_G)	15-30 nm	15-30 nm
Underlap S/D (L_{US}, L_{UD})	5 nm	5 nm
Molefraction (x)	0.25	0.25
Total Device Length (L_T)	110 nm	110 nm
Total Device Width (L_W)	32 nm	32 nm

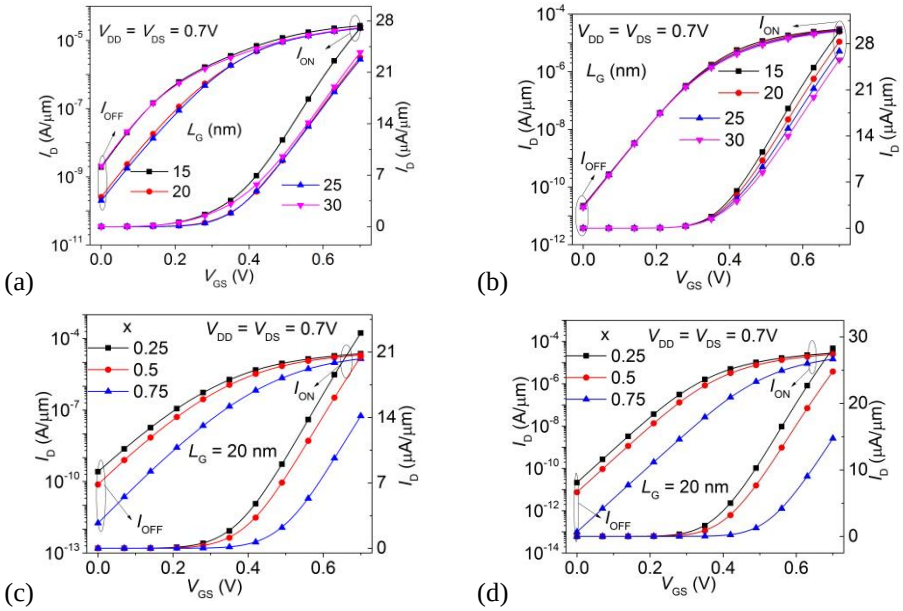

Fig. 2 Transfer characteristics of (a) JL FinFET and (b) Wavy-JL FinFET for varying L_G = 15-30 nm at N_D = 1.7 x10^{19} cm^{-3}, ϕ_M = 4.6 eV.

As shown in Fig. 2a and 2b, the I_D-V_{GS} is plotted in logarithmic and linear scales, an improvement in I_{ON} and I_{OFF} is observed for Wavy-JL FinFET. The device layer (S/D and channel) is $Si_{1-x}Ge_x$ material with molefraction x = 0.25. Considering x = 0.25,

substituting this value of x, results in high content of Si in SiGe material. Therefore, the device acquires the properties of Si material, and accordingly the simulation data are extracted. The conduction mechanism of JLT seems to be similar to that of IM devices, JL device with no concentration gradients across the S/D channel regions and high N–type doping profile induces a volume inversion mechanism. From the Fig. 2 it is analyzed that, as the L_G is scaled down, the I_{ON} enhances and I_{OFF} reduces, on this point of view the performance of the device is identified using SiGe channel. In Fig. 2C and 2D the I_D is plotted along the V_{GS} for the different value of x at L_G = 20 nm, from this it is realized that as the value of x increases the shift in V_{TH} takes place which there reduces the I_{OFF}.

3. RESULTS AND DISCUSSIONS

The section deals with the results and discussions carried out for the simulation study. The higher order g_m of I_D characteristics results in the second and third order ($g^{\backslash}_m$, $g^{\backslash\backslash}_m$) parameters. Further, these parameters result in second and third order intermodulation and linearity performances. In MOS circuits, harmonic distortion occurs due to the nonlinearity exhibited by higher-order derivatives of I_D-V_{GS} characteristics. Therefore, the circuits realize balanced topologies, due to this the even-order harmonics are cancelled out. The third order harmonic, which represents $g^{\backslash\backslash}_m$, determines a lower limit of distortion and hence amplitude should be minimized. Thus, reducing $g^{\backslash\backslash}_m$ and increasing the g_m acts as a sustainable solution to improve device linearity[31].

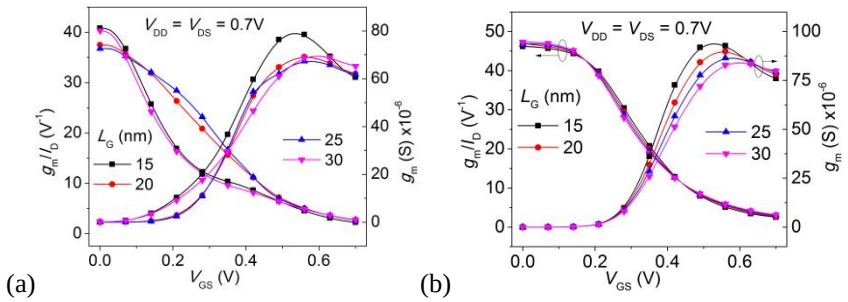

Fig. 3 *TGF* and g_m as a function V_{GS} (a) JL FinFET and (b) Wavy-JL FinFET for different L_G = 15-30 nm at N_D = 1.7 x10^{19} cm^{-3}, ϕ_M = 4.6 eV and x = 0.25.

The Fig. 3 represents *TGF* (g_m/I_D) and g_m the values are extracted from the measured values of I_D and plotted as a function of V_{GS} as illustrated in Fig. 2(a, b). The graphs exhibit different dimensions of L_G, JL transistors, and show that a lower g_m is induced at room temperature because of the reduced carrier mobility with that of the IM devices. The mobility is an important parameter for evaluating g_m, but the other factors may also affect this parameter. According to the drift equation the current that flows through the device layer has a great impact on the mobility, E-Field, and N_D. This can be identified without including the mobility degradation models to the simulator and measured at different dimensions. The parameter *TGF* is observed as the available gain per unit value of power dissipation. From the Fig. 3 g_m increases as the I_D increases for scaled L_G, but

the *TGF* decreases as the L_G scales down. However, the *TGF* values are near to the ideal values and but the g_m values are very high for JL FinFET.

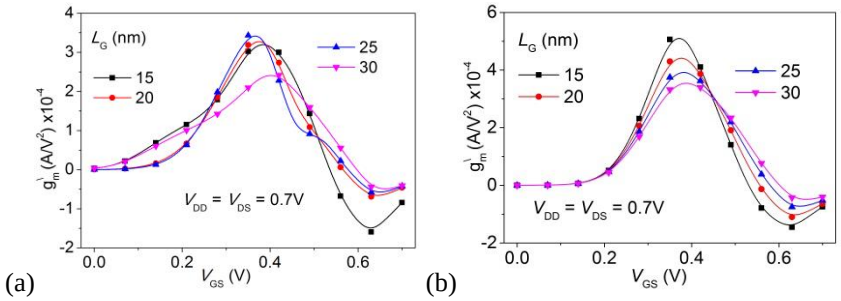

Fig. 4 $g^{\backslash}_m$ as a function V_{GS} (a) JL FinFET and (b) Wavy-JL FinFET for different L_G = 15-30 nm at N_D = 1.7 x10^{19} cm^{-3}, ϕ_M = 4.6 eV and x = 0.25.

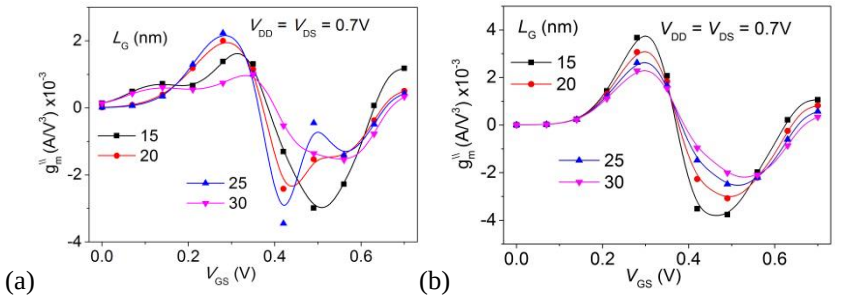

Fig. 5 $g^{\backslash\backslash}_m$ as a function V_{GS} (a) JL FinFET and (b) Wavy-JL FinFET for different L_G = 15-30 nm at N_D = 1.7 x10^{19} cm^{-3}, ϕ_M = 4.6 eV and x = 0.25.

Table 2 SC parameters 3D JL FinFET at V_{DS} = 0.7V.

L_G (nm)	S-Ssub (mV/decade)	I_{ON} x10^{-5} (A/μm)	I_{OFF} x10^{-10} (A/μm)
15	70.446	2.70	0.190
20	80.12	2.30	2.57
25	81.419	2.28	2.01
30	70.905	2.37	0.20

Table 3 SC parameters for Wavy-JL FinFET at V_{DS} = 0.7V.

L_G (nm)	S-Ssub (mV/decade)	I_{ON} x10^{-5} (A/μm)	I_{OFF} x10^{-11} (A/μm)
15	66.702	2.99	2.24
20	66.545	2.83	2.12
25	66.427	2.69	2.02
30	66.357	2.55	1.94

Table 4 SC parameters at different values of X for JL FinFET V_{DS} = 0.7V, L_G = 20 nm.

X	S-Ssub (mV/decade)	I_{ON} x10^{-5} (A/μm)	I_{OFF} (A/μm)
0.25	80.12	2.30	2.57x10^{-10}
0.5	78.662	2.05	7.48x10^{-11}
0.75	77.449	1.42	1.79x10^{-12}

Table 5 SC parameters at different values of X for 3D Wavy-JL FinFET V_{DS} = 0.7V, L_G = 20 nm.

X	S-Ssub (mV/decade)	I_{ON} x10^{-5} (A/μm)	I_{OFF} (A/μm)
0.25	66.545	2.83	2.12 x10^{-11}
0.5	66.89	2.48	7.44 x10^{-12}
0.75	67.319	1.47	9.88 x10^{-14}

The higher order derivatives of I_D ($g^{\backslash}_m$ and $g^{\backslash\backslash}_m$) as a function V_{GS} for different L_G at V_{DS} = 0.7 V are plotted in Fig. 4 and 5 respectively. Usually for better linearity properties there should be a lesser distortion amplitude of $g^{\backslash}_m$ and $g^{\backslash\backslash}_m$. The value of V_{GS} at which the higher order of transconductance parameters ($g^{\backslash}_m$ and $g^{\backslash\backslash}_m$) becomes zero is known as zero crossover point (*ZCP*) which decides the optimum bias point for device operation [15], [32]. Therefore, from the Fig. 4 and Fig. 5 the minimal higher order derivative shows better for Wavy-JL FinFET.

The comparison of SC parameters for JLT devices at L_G variation is tabulated in Tables 2 and 3, and at fixed L_G with different values of x is given in Table 4 and 5. From the overall simulation study the Wavy- JLT explores good improvement in I_{ON} and possess less sensitivity to SCEs over the conventional one.

4. CONCLUSION

The paper investigates the performance study of analog analysis and higher order parameters for both conventional and Wavy JLFinFET for different L_G variations. Due to the equal amount of doping profiles along the device layer the I_{ON} is improved and I_{OFF} is decreased. The conduction mechanism of JL FinFET with the concept of SiGe device layer is explained at different values of x. The simulation results are extracted at V_{DSAT} values at x = 0.25, ϕ_M = 4.6 eV are considered to estimate the I_D characteristics and the higher order parameters are evaluated accordingly. From the results it has been observed that the higher order parameters show minimal non-linearity distortions performance for Wavy-JL FinFETs over conventional JLT. Therefore, the performance of the 3D Wavy-JL FinFET shows better channel controllability through gate and thereby enhances the I_D. On the other hand, the high N_D with the effective channel length and width of the depletion layer are also responsible to achieve scaled SCEs.

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