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DESIGN OF NOVEL EFFICIENT FULL ADDER CIRCUIT FOR QUANTUM-DOT CELLULAR AUTOMATA TECHNOLOGY

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Abstract. *In this paper the novel coplanar circuits for full adder implementation in Quantum-dot Cellular Automata (QCA) technology are presented. We propose a novel one-bit full adder circuit and then utilize this new circuit to implement novel four-bit Ripple Carry Adder (RCA) circuit in the QCA technology. The QCADesigner tool version 2.0.1 is utilized to implement the designed QCA full adder circuits. The implementation results show that the designed QCA full adder circuits have an improvement compared to other QCA full adder circuits.*

Key words: *Full adder, quantum-dot cellular automata, coplanar circuit, ripple carry adder, high-performance design*

1. INTRODUCTION

Computer arithmetic plays an important role in the information and communication applications such as cryptography and ALU [1-3]. Full adders have an important role in computer arithmetic. So, the efficiency of many computer arithmetic applications is primarily determined by the efficiency of the full adder implementation [1-3].

On the other hand, Quantum-dot Cellular Automata (QCA) technology is a promising technology, which can continue the Moore's law development. This technology uses charge formation to information transition instead of current. As a result, circuit design in the QCA technology has advantages in comparison with conventional technologies such as CMOS technology in terms of small dimension, fast operation and low power consumption [4, 5].

Recently, several efforts have been done to improve the efficiency of the full adder implementation in the QCA technology [6-15]. Hänninen and Takala [6] presented a QCA full adder that requires 102 QCA cells and 0.1 μm^2 area. Ramesh and Rani [7]

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designed a QCA full adder that consists of 52 QCA cells and 0.038 μm^2 area. Abedi et al. [8] designed a QCA full adder that requires 59 QCA cells and 0.043 μm^2 area. Hashemi, and Navi [9] have offered a QCA full adder that requires 71 cells and 0.06 μm^2 area. Mohammadi et al. [10] presented a QCA full adder that requires 38 QCA cells and 0.02 μm^2 area. Ahmad et al. [11] constructed a QCA full adder that consists of 41 QCA cells and 0.04 μm^2 area. Labrado and Thapliyal [12] have presented a QCA full adder that requires 63 QCA cells and 0.05 μm^2 area. Balali et al. [13] designed a QCA full adder that requires 29 QCA cells and 0.02 μm^2 area. However, these full adder circuits have advantages, but the complexity and required area of full adder circuit in the QCA technology can be reduced with a described new technique in this paper.

In this paper, an efficient circuit for one-bit QCA full adder is presented and evaluated. Then, an efficient circuit is designed for four-bit QCA Ripple Carry Adder (RCA). The functionality of the designed circuits is verified using QCADesigner tool version 2.0.1. The implementation results show that the designed circuits have advantages compared to recent modified one-bit QCA full adder circuits and four-bit QCA RCA circuits.

The rest of this paper is organized as follows. Background of the developed circuits is presented in section 2. The designed circuits are presented in section 3. Section 4, evaluates the designed circuits. Finally, section 5 concludes this paper.

2. BACKGROUND

2.1. QCA technology

QCA technology is an emerging technology that can utilize for development of digital circuits based on Moore's law. This new technology utilizes the charge formation instead current for information transition. The basic element in this technology is a four dots square, which has two free electrons. Fig. 1 shows a simplified QCA cell [1, 5].

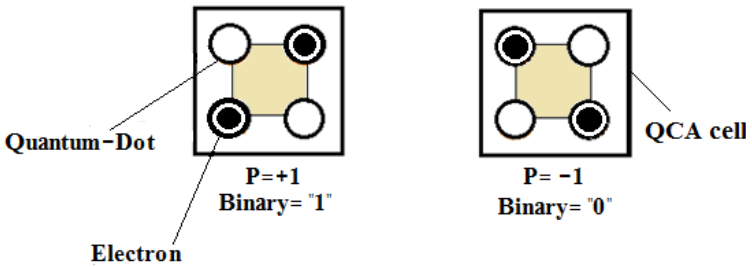

Fig. 1 A simplified QCA cell [1, 5]

The formation of these free electrons is utilized to denote the zero state and one state logic in this technology. Using this cell, the logic elements such as majority gate [4] can be developed.

It should be noted that other logic elements such as OR gate and AND gate can be developed using majority gate [1, 4, 5]. Moreover, complex digital circuits such as full adder circuits [6-15] and multiplexer circuits [1, 5] are developed using these logic elements.

2.2. QCA full adder circuit

Full adder plays a vital role in the complex digital circuits. As a result, high-performance implementation of this circuit is an attractive research area. The logical function of one-bit full adder can be shown by following equation:

$$\text{Carry} = AB + AC_{in} + BC_{in} = \text{Maj}\,3\,(A, B, C_{in}) \tag{1}$$

$$\text{Sum} = A \oplus B \oplus C_{in} = \text{Maj3}(C_{in}, \text{Maj3}\,(A, B, \overline{C}_{in}), \overline{\text{Carry}}) \tag{2}$$

In (1) and (2), A, and B denote the inputs of one-bit full adder. C_{in} and Carry denote the carry input and carry output, respectively. Sum denotes the output of sum in the one-bit full adder. Moreover, Maj3 denotes the 3-input majority function, which can be implemented using 3-input majority gate in the QCA technology [1, 4, 9]. Fig. 2 shows the circuit diagram for the one-bit QCA full adder [6-9].

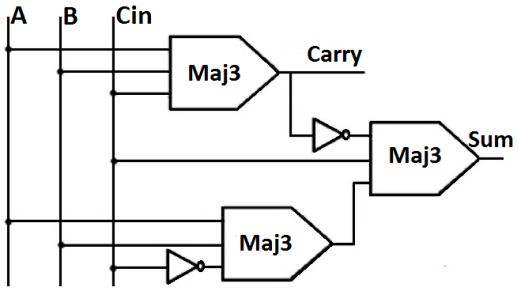

Fig. 2 The circuit diagram for the one-bit QCA full adder [6]

In addition, the four-bit QCA RCA circuit can be achieved by using consecutively four one-bit full adder [1, 6-9]. Fig 3 shows the four-bit QCA RCA circuit.

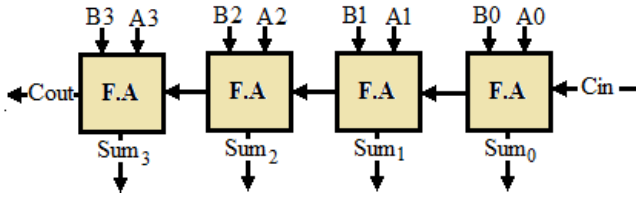

Fig. 3 The four-bit QCA RCA circuit [6]

In this circuit, A = (A_3, A_2, A_1, A_0), B = (B_3, B_2, B_1, B_0) are two four-bit inputs. The C_{in} and C_{out} denote the one-bit carry input and carry output, and Sum = (Sum_3, Sum_2, Sum_1, Sum_0) is four-bit output.

3. THE DESIGNED QCA CIRCUITS

This section outlines a novel one-bit QCA full adder circuit. Then, the new four-bit QCA RCA circuit is designed based on the designed one-bit QCA full adder circuit.

3.1. The designed QCA full adder circuit

The designed circuit for the one-bit QCA full adder circuit is shown in Fig. 4.

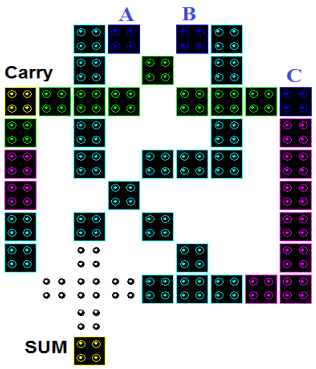

Fig. 4 The designed circuit for the one-bit QCA full adder

In this circuit, A and B are two one-bit inputs and C is the carry input. Carry and SUM denote the outputs of carry and sum, respectively. This circuit consists of 46 QCA cells. Note that, four clocking zones are utilized in this circuit as follows: white indicates clock zone 3, light blue indicates clock zone 2, violet indicates clock zone 1, and green indicates clock zone 0.

3.2. The designed QCA RCA circuit

The designed circuit for the four-bit QCA RCA circuit is shown in Fig. 5.

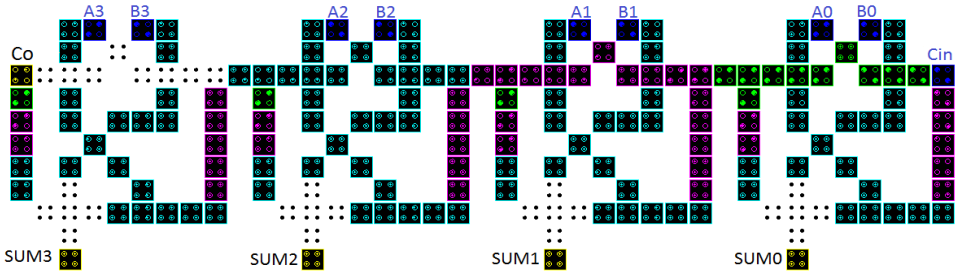

Fig. 5 The designed circuit for the four-bit QCA RCA

In this circuit, A and B are two four-bit inputs and C_{in} is the one-bit carry input. Carry and SUM denote the outputs of one-bit carry and four-bit sum, respectively. This circuit consists of 187 QCA cells.

4. IMPLEMENTATION RESULTS AND COMPARISON

The designed circuits are implemented using QCADesigner tool version 2.0.1. This section presents these implementation results.

4.1. The designed QCA full adder circuit

Fig. 6 shows the implementation results of the designed circuit for the one-bit QCA full adder.

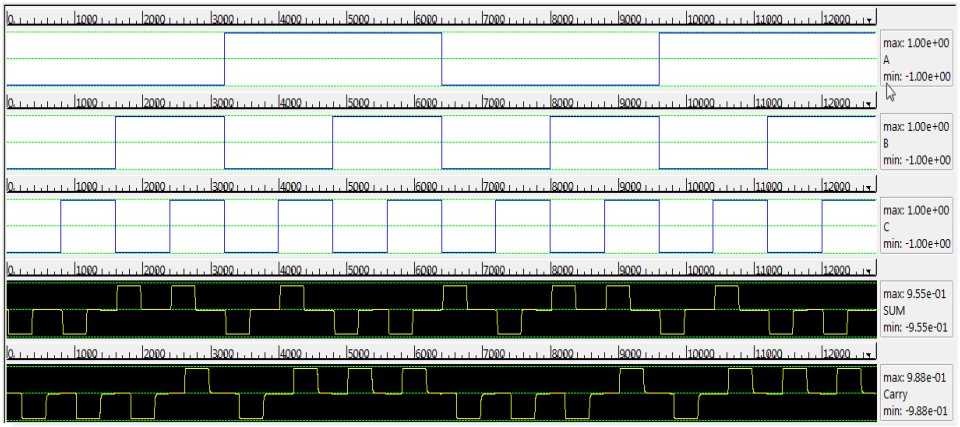

Fig. 6 The implementation results for the designed one-bit QCA full adder circuit

The implementation results of the designed circuit for the one-bit QCA full adder confirm the correctness of this circuit. Table 1 summarizes the implementation results of the designed circuit for the one-bit QCA full adder compared to other one-bit QCA full adder circuits in [6-13].

Table 1 The comparative table for one-bit QCA full adder circuits

Reference	Complexity (#cell)	Area (μm^2)	Delay (clock zone)
[6]	102	0.1	8
[9]	71	0.06	5
[7]	52	0.038	4
[8]	59	0.043	4
[10]	38	0.02	3
[11]	41	0.04	2
[12]	63	0.05	3
[13]	29	0.02	2
This paper	46	0.04	4

Based on our implementation results that are shown in Fig. 6 and Table 1, the designed circuit for the one-bit QCA full adder has an improvement in terms of complexity compared to other one-bit QCA full adder circuits in [6-9, 12]. Although the cell count in one-bit QCA

full adder circuits in [10, 11, 13] is lower than our designed one-bit QCA full adder circuit, our designed four-bit QCA RCA circuit, which is utilized this one-bit QCA full adder circuit as its basic block, has advantages compared to four-bit QCA RCA circuits in [10, 13]. It is because the input/output ports in the developed one-bit QCA full adder have suitable places. So, the place and route results in the developed four-bit QCA RCA presents a better results. Moreover, the output cells of one-bit QCA full adder circuit in [11] aren't suitable placed. So, the implementation of four-bit QCA RCA circuit using the one-bit QCA full adder circuit in [11] is hard.

4.2. The designed QCA RCA circuit

Fig. 7 shows the implementation results of the designed circuit for the four-bit QCA RCA.

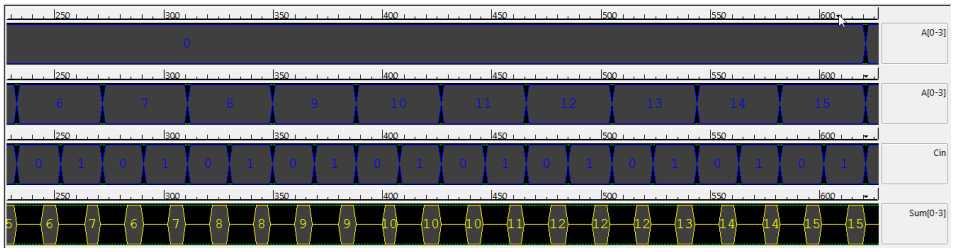

Fig. 7 The implementation results for the designed the four-bit QCA RCA circuit

The implementation results of the designed circuit for the four-bit QCA RCA confirm the correctness of this circuit. Table 2 summarizes the implementation results of the designed circuit for the four-bit QCA RCA compared to other four-bit QCA RCA circuits in [6-10, 12-14].

Table 2 The comparative table for four-bit QCA RCA circuit

Reference	Complexity (#cell)	Area (μm^2)	Delay (clock zone)
[6]	558	0.85	20
[9]	442	1	8
[7]	260	0.28	10
[8]	262	0.208	28
[10]	237	0.24	6
[12]	295	0.3	6
[13]	269	0.37	14
[14]	339	0.2542	7
This paper	187	0.2	16

Based on our implementation results that are shown in Fig. 7 and Table 2, the designed circuit for the four-bit QCA RCA has an improvement in terms of complexity, and area compared to other four-bit QCA RCA circuits in [6-10, 12-14].

5. CONCLUSION

Full adders play an important role in computer arithmetic fields. So, efficient implementation of full adders can increase the efficiency of the computer arithmetic circuits. This paper presented and evaluated an efficient full adder circuit in the QCA technology. In addition, we implemented a four-bit QCA RCA circuit based on this new one-bit QCA full adder. The designed circuits have been implemented using QCADesigner tool version 2.0.1. The implementation results confirmed that the designed circuits outperform recent modified one-bit QCA full adder circuits and four-bit QCA RCA circuits in [6-9, 12] in terms of complexity, and required area.

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