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Original scientific paper

AREA AND POWER-EFFICIENT RECONFIGURABLE DIGITAL DOWN CONVERTER ON FPGA

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Abstract. *This paper presents a field-programmable gate array (FPGA)-based digital down converter (DDC) that can reduce the bandwidth from about 70 MHz to 182.292 kHz. The proposed DDC consists of a polyphase COordinate Rotation DIgital Computer (CORDIC) processor and a multirate filter. The advantage of polyphase CORDIC processor is to process with high sample rate input data and produces computational efficient noiseless baseband spectrum. The pipeline multirate filter works at a high clock speed. Moreover, the multirate filter generates a fractional sample rate factor using a cubic B-spline Farrow filter. The proposed DDC is coded with optimal hardware description language (HDL) and tested on Kintex-7 Xilinx FPGA as the target device. Experimental results indicate that the proposed design saves chip area, power consumption and operates at high speed without loss of any functionality. Additionally, the proposed design offers sufficient spurious-free dynamic range (SFDR) and produces less than 1 Hz frequency resolution at the output.*

Key words: *Digital down converter (DDC), COordinate Rotation DIgital Computer (CORDIC), Half-band (HB) filter, Field programmable gate array (FPGA), MATLAB*

1. INTRODUCTION

The demand for a high-performance digital down converter (DDC) is very much essential in modern communication [1]. The sample rate reduction process plays an important role in data communication systems for its various data rates. Hence, field-programmable gate array (FPGA)-based DDC architecture is very much essential due to its outstanding flexible architecture as compared to application-specific integrated circuits (ASIC) [2]. Furthermore, the implementation of DDC on FPGA performs superbly in frequency response and phase characteristics with a high precision output.

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In the last decade, several researchers have reported hardware-efficient different DDC architectures on FPGA devices. Recently, the authors in L. L. Motta et al. [3] have proposed a digital up-down converter using polyphase cascaded integrated comb (CIC) filters. The simulation results show the functional verification of the filters, and the design has achieved a high performance using fixed-point filter coefficients. Again, L. Guo et al. [4] have suggested parallel DDC architecture using numerical control oscillator (NCO). The NCO was decomposed into several sinusoidal sequences. These sequences are multiplied by the input signals to produce complex waveforms. The design was verified by MATLAB and tested on the FPGA board. Similarly, the authors in X. Liu et al. [5] proposed a reconfigurable DDC architecture that performed a down-converted signal about 3.6 GHz to the output range of 1 kS/s-225 MS/s. The design was implemented on the Xilinx Kintex-7 device and measured the synthesized results in terms of resources and power consumption. Furthermore, the authors in B. Tietche et al. [6] described FPGA-based resampling circuits for software-defined radio applications. The implementation schemes controlled the spurious-free dynamic range (SFDR). Again, the authors in V. Obradović et al. [7] discussed a flexible DDC architecture for wideband direction finder. The DDC was tested on Xilinx Kintex-7 using Xilinx IP cores to implement the filters chain. Similarly, authors in J. Thabet et al. [8] presented a reconfigurable DDC design implemented on Virtex-7 FPGA board to obtain high speed, low power consumption. The design reduced the complexity for applicability in multi-standard GNSS receivers. Furthermore, the authors in A. Agarwal et al. [9] suggested COordinate Rotation DIgital Computer (CORDIC)-based DDC on Xilinx Virtex-6 FPGA for multi-standard radio communications and achieved a maximum operating speed of 240 MHz. However, all the existing designs have some drawbacks in hardware implementation. They consume a large area and power in the FPGA platform. Thereby a cost-efficient reconfigurable DDC architecture is very much attractive in a communication system.

Therefore, hardware efficient flexible DDC architecture is required that can meet all the practical applications. The proposed design uses a polyphase and pipelined architecture to improve the operating speed. Again, the truncation process in each unit reduces the area requirements. Finally, the proposed design is tested on the Xilinx Kintex-7 FPGA board. The implementation results indicate that the proposed DDC optimizes the hardware resources and power as compared to existing architectures without losing any significant information. The organization of this paper is as follows: Section 2 describes the proposed architecture and its components. Results are discussed in Section 3. Section 4 concludes the paper.

2. Proposed Architecture

The proposed DDC consists of a polyphase CORDIC processor and multirate filter, as shown in Fig. 1. The polyphase CORDIC processor works a high data rate input signal which is beyond 1 GHz. The multirate filter such as multi-stage CIC, half-band (HB), and cubic B-spline Farrow filters are connected in cascade to achieve a high decimation factor and to the produce correct baseband spectrum.

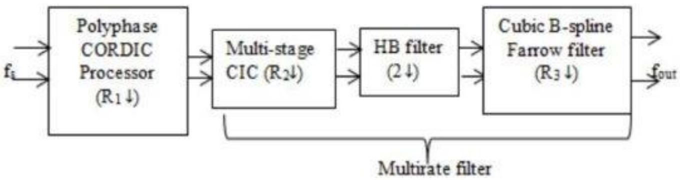

Fig. 1 Proposed DDC architecture

The total sample rate (R) factor is calculated as

$$R = f_{out} / f_s = R_1 \times R_2 \times 2 \times R_3 \tag{1}$$

Where f_s and f_{out} is the input and output sampling rate, respectively. R_1 is the decimation factor of the polyphase CORDIC processor, R_2 is the decimation factor of the multi-stage CIC filter, R_3 is the decimation factor of the cubic B-spline Farrow filter.

The sample rate factors can be changed dynamically in real-time to match any practical application. Hence, the design offers maximum flexibility. The frequency resolution at the output is $f_s/2^{32}$ (= 0.8381Hz for f_s = 3.6 GHz).

The following sub-modules describe each component of the proposed design.

2.1. Polyphase CORDIC Processor

The polyphase CORDIC processor can satisfactorily work with a high sample rate signal which is the output from an analog-to-digital (ADC) converter (typically, ADC12D1800). The proposed polyphase CORDIC processor is shown in Fig. 2. The polyphase component operates at a speed of f_s/R_1, resulting in the polyphase CORDIC processor being more feasible in the FPGA platform [10]. To achieve correct output, the relation between f_s and R_1 is expressed as

$$R_1 \le f_s/W \tag{2}$$

Where W is bandwidth of the input signal.

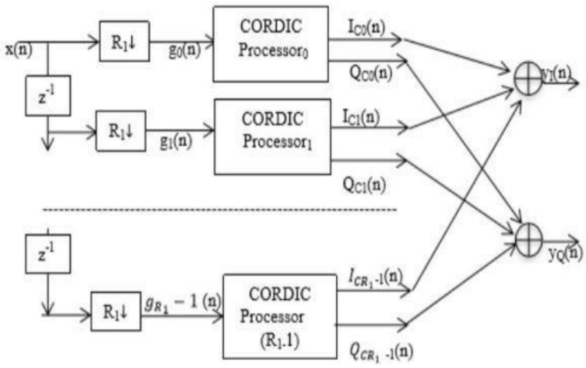

Fig. 2 Polyphase CORDIC processor

From the polyphase algorithm, the signal $g_i(n)$ can be represented as

$$g_i(n) = x(nR_1 + i) \tag{3}$$

Where i = 0, 1, ………… (R_1-1), and x(n) is the input sequence.

Hence, the in-phase ($y_I(n)$) and quadrature ($y_Q(n)$) parts of the polyphase CORDIC processor are expressed as [11]

$$y_I(n) = \sum_{i=0}^{R_1-1}[g_i(n)I_{Ci}(n)]$$
$$= \sum_{i=0}^{R_1-1}[x_i(nR_1+i)\cos[2\pi(nR_1+i)f_0/f_s] \tag{4}$$

and

$$y_Q(n) = \sum_{i=0}^{R_1-1}[x_i(n)Q_{Ci}(n)] \tag{5}$$
$$= \sum_{i=0}^{R_1-1}[x_i(nR_1+i)\sin[2\pi(nR_1+i)f_0/f_s] \text{ respectively}$$

Where f_o is the central frequency. To eliminate unwanted frequency components and further reduce the sample rate to ensure a correct output signal, both $y_I(n)$ and $y_Q(n)$ signals are passed through multirate decimation filters.

2.2. CIC Filter

The CIC filter performs low-pass filtering to remove the multiple copies of images and produces a very narrow passband for the DDC system [12]. CIC is a high efficient decimation filter that is placed just after the polyphase CORDIC processor. A multi-stage CIC filter is typically used to reduce the sidelobe producing maximum main lobe gain [13]. This work allows a pipeline 4-stage CIC decimation filter, shown in Fig. 3. The additional register in the integrator and comb section reduces critical path delay.

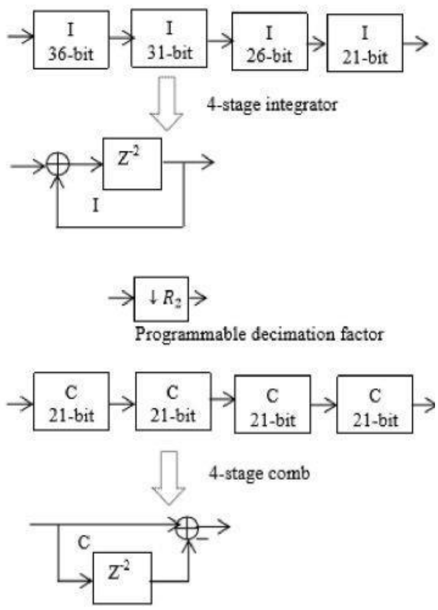

Fig. 3 4-stage truncated pipeline-based CIC filter

The filter gain is calculated as [14]

$$G = (R_2D)^N = 65536 \text{ (For } R_2 = 8\text{, stage N = 4, and comb delay D = 2)} = 48.16 \text{ dB} \tag{6}$$

The full resolution data width at the output stage is

$$B_{out} = [B_{in} + \mathrm{N}log_2(R_2 D)] = 36 \text{ bits } \ [B_{in} = 20] \tag{7}$$

Fig. 4 depicts the magnitude response of the CIC filter.

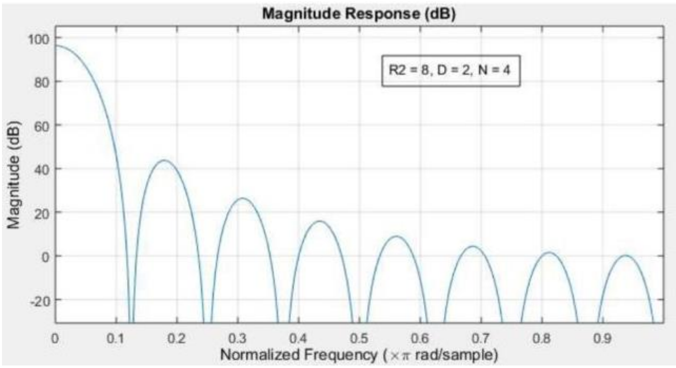

Fig. 4 Magnitude response of the CIC filter for $R_2 = 8$, D = 2, N = 4

Generally, integrator works at a high sample rate with a large data width. Hence, the truncation process is necessary to reduce the word length without losing desired information. It is noted that the five least significant bits (LSBs) are truncated from the first integrator's 36-bit. Hence, the second integrator works only 31-bit. Using the same procedure, the third and fourth integrators are work only with 26-bit and 21-bit, respectively. As a consequence, the truncation process reduces the output data width to 16-bit. Usually, the Matlab tool provides the data length in each stage. The passband frequency (ω_p) is $\pi/\mathrm{N}\,R_2$.

2.3. HB Filter

It is important to note that the CIC filter does not provide a flat response and its non-flatness must be compensated in other processing stages. After the CIC filter, the HB filter is used to attain the correct passband droop [15]. The HB filter has symmetric property at cut-off frequency π/2. Fig. 5 shows a 31-tap symmetric HB filter with decimation factor 2.

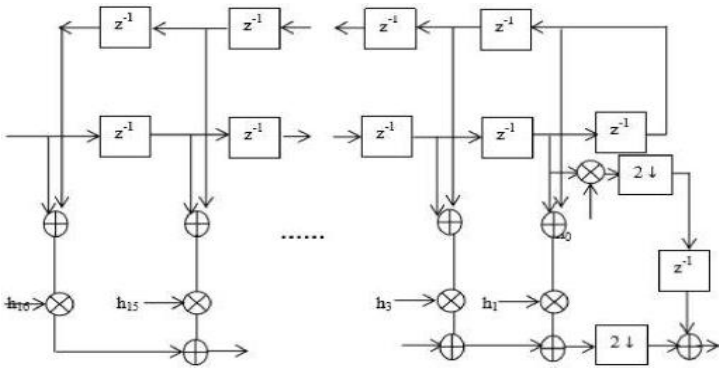

Fig. 5 31-tap transpose symmetric HB filter

The pass-band frequency (ω_p) is 0.45π, and stop-band frequency (ω_s) is 0.55π. The transpose symmetric HB architecture reduces the multiplication units [16]. Hence, the computational workload reduces significantly. For this work, the HB filter coefficients are 16-bit fixed points and generated using the "firhalfband" Matlab function [17].

2.4. Cubic B-spline Farrow structure

Finally, a cubic B-spline Farrow structure is used to produce the fractional sampling output with 3/2 times the input signal. This type of implementation provides a better reconstruction of the signal as compared with conventional Lagrange interpolation [18], [19]. The calculation of the cubic B-spline Farrow structure is described below.

The Nth degree B-spline at time domain is expressed as [14]

$$\beta^N(t) = \frac{1}{N!}\sum_{k=0}^{N+1}(-1)^k \binom{N+1}{k}\left(t - k + \frac{N+1}{2}\right)^N \tag{8}$$

Where β^N represents as N-th B-spline. Consider, N = 3, or cubic spline type, then the polynomial becomes

$$\beta^3(t) = \frac{1}{6}\sum_{k=0}^{4}(-1)^k \binom{4}{k}\,(t - k + 2)^3 \tag{9}$$

$$= \frac{1}{6}(t+2)^3 - \frac{2}{3}(t+1)^3 + t^3 - \frac{2}{3}(t-1)^3 + \frac{1}{6}(t-2)^3 \tag{10}$$

The reconstruction spline is the summation of weighted B-spline sequences and expressed as

$$y(t) = \sum_k x(k)\beta^3(t-k) \tag{11}$$

Consider, the samples are taken at time t = -1, 0, 1, 2, and from Eq. (11), the four parts B-splines are calculated as

$$y(d) = x(n+2)\,\beta^3(d-2) + x(n+1)\,\beta^3(d-1) + x(n)\,\beta^3(d) + x(n-1)\,\beta^3(d+1)$$

$$= x(n+2)\frac{d^3}{6} + x(n+1)\left[\frac{1}{6}(d+1)^3 - \frac{2}{3}d^3\right] + x(n)\left[d^3 - \frac{2}{3}(d+1)^3 + \frac{1}{6}(d+2)^3\right] + x(n-1)\left[-\frac{1}{6}(d-1)^3\right]$$

$$= x(n+2)\frac{d^3}{6} + x(n+1)\left[-\frac{d^3}{2} + \frac{d^2}{2} + \frac{d}{2} + \frac{1}{6}\right] + x(n)\left[\frac{d^3}{2} - d^2 + \frac{2}{3}\right] + x(n-1)\left[-\frac{d^3}{2} + \frac{d^2}{2} - \frac{d}{2} + \frac{1}{6}\right] \tag{12}$$

For realizing the above equations in Farrow structure, the factors of fractional delay d^k are generated by the following four equations:

$$\begin{array}{llllll}
d^0: & 0 & + x(n+1)/6 & + 2x(n)/3 & + x(n-1)/6 & = C_0 \\
d^1: & 0 & + x(n+1)/2 & + 0 & - x(n-1)/2 & = C_1 \\
d^2: & 0 & + x(n+1)/2 & - x(n) & + x(n-1)/2 & = C_2 \\
d^3: & x(n+2)/6 & - x(n+1)/2 & + x(n)/2 & - x(n-1)/6 & = C_3
\end{array} \tag{13}$$

Where C_0, C_1, C_2, and C_3 are represented as spline matrix coefficients and d lies between 1 and 0. The above coefficients in Eq. (13) are transformed into z-domain to realize the transfer functions of the Farrow filter architecture, as shown in Fig. 6. Farrow filters are the most suitable architecture for fractional sample rate converter due to its one programmable fractional delay component without changing filter coefficients [19].

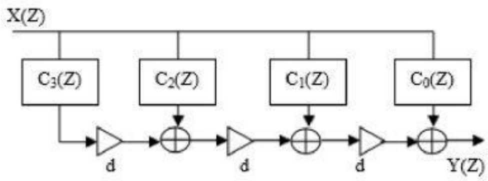

Fig. 6 Cubic B-spline Farrow structure [20]

3. Result Analysis

The following sub-sections describe the result analysis in detail.

3.1. Design Specifications

The proposed system performs for mobile communication specifications. All floating-point data are converted to fix-point data to achieve stopband specifications. The specifications of the proposed DDC are summarized as follows:

i. Input signal bandwidth: 70 MHz.
ii. Output signal bandwidth: 182.292 kHz
iii. Decimation factor: 384 (R_1=4, R_2=2^5, HB =2, R_3=3/2)
iv. Input data width: 16-bit
v. Output data width: 20-bit
vi. Passband ripple $\leq$ 0.1 dB
vii. Stopband attenuation $\geq$ 80 dB

3.2. Data Truncation

The truncation is applied in each signal path to protect overflow error. Each polyphase branch can be represented as an FIR filter. The multiplication-accumulation is described as follows. An M-bit binary word signifies in signed 2's complement fixed-point rational format and can take value from subset S as [21]

$$S = \{s/2^{y_1} | -2^{M-1} \leq s \leq 2^{M-1} - 1, s \in Z\} \quad (14)$$

Which is represented as P (x_1, y_1), where $x_1 = M - y_1 - 1$ and y_1 fractional bits. Using fixed-point arithmetic, the multiplication is calculated as

$$P(x_1, y_1) \text{ x } P(x_2, y_2) = P(x_2 + x_2 + 1, y_1 + y_2) \text{ or } P(x_3, y_3) \quad (15)$$

Consider, the multiplication and accumulation are denoted by P (x_3, y_3) and P (x_4, y_4), respectively, so that

$$P(x_4, y_4) = A(x_3 + \text{floor}[\log_2(R-1)], y_3) \quad [\text{Where } R = R_1 + 1] \quad (16)$$

For example, the input data is P (8, 7), and the coefficient data is A (3, 12). Hence, the multiplication and accumulation data are P (12, 19) and P (14, 19) respectively [for R_1 = 4]. According to the word length reduction, the output data is P (14, 19–14) or A (14, 5) or data word length (14 + 5 + 1) 20-bit which are the input of the CIC filter. The output word lengths of the CIC filter are 16-bit [described in section 2.3]. Again, the Farrow FIR output word length is 20-bit.

3.3. FPGA Implementation

The proposed DDC design is simulated in Xilinx Vivado 2017.4 tool and implemented on Kintex-7 XC7K70T-FBG676 with 16-bit input precision to meet the desired specifications. The design is coded using Verilog hardware description language (HDL). Additionally, the code optimization technique reduces the logical resources and power [22], [23]. The compilation report contains Slices, LUTs, IOB blocks, maximum frequency, and power consumption. Table 1 indicates the synthesized list of each component of the proposed design.

Table 1 Resource utilization of each component of the proposed DDC architecture

Synthesis parameters	Polyphaser CORDIC processor			CIC filter	HB filter (31-tap)	Cubic B-spline Farrow filter
	R_1=4	R_1=8	R_1=16	($R_2 = 2^5$)	(2)	($R_3 = 3/2$)
Slice Registers	1758	3650	8521	1290	1948	3182
6-input LUTs	832	1975	3932	556	878	2185
IOBs	62	62	62	65	80	86
BRAMs	2	4	8	0	0	8
DSP48Es	4	8	16	0	0	36

3.4. Validation

For the purpose of verification, ChipScope outputs are sent back in the Matlab R2015a tool. Fig. 7 shows SFDR of 88 dB, which can be generated using 1024 samples with unity signal amplitude.

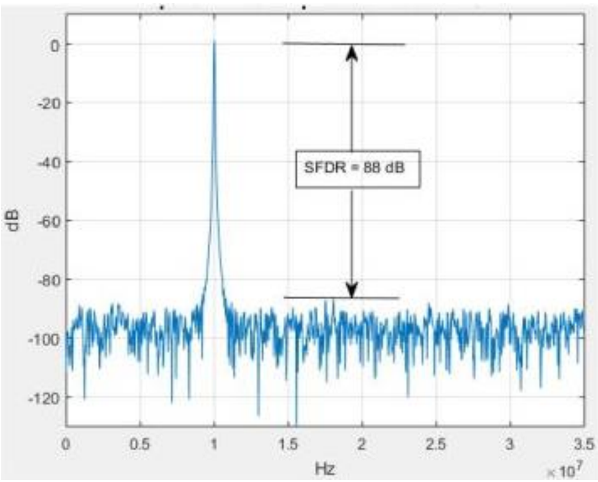

Fig. 7 Power spectrum of proposed DDC

3.5. Comparison

Table 2 shows a comparison report of the proposed DDC design with the existing designs. The proposed design uses data truncation to reduce the resources. This area reduction leads to power optimization. Moreover, the pipeline version of this proposed architecture enhances the operating speed. The area and power are reduced by 39.65% and 32.92%, respectively. The polyphase CORDIC processor improves the SFDR, which is 88 dB. Results analysis suggested that the proposed DDC is an energy-efficient architecture that is widely used in real-time signal processing applications.

Table 2 Comparison report of existing architectures and proposed solution

Synthesis parameters	Vuk et al. [7] (Kintex-7) f_s = 120 MHz R = 6	Liu et al. [5] (Kintex-7) f_s = 3.6 GHz R = 20	Proposed solution
Slices	37066	13552	8178
LUTs	69499	7269	4451
BRAMs	Not available	22	10
DSP48Es	1034	83	40
F_{max} (MHz)	Not available	454.5	512
Power (W)	Not available	1.446	0.970
SFDR (dB)	Not available	83.3	88

4. CONCLUSION

This paper briefs an FPGA-based flexible DDC architecture so that it can match any digital radio specifications. The proposed design uses a polyphase and pipelined structure which can save the area and improve the operating speed. The multirate filter performs sample rate reduction and channel filtering with enhanced sensitivity and selectivity. These new design techniques increase the operating speed. Furthermore, the truncation and optimum coding style are used to improve area efficiency and power reduction. Additionally, the proposed design has achieved an SFDR of 88 dB. Thus, the presented DDC design has been enhanced in real-time applications.

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