i-ETC: ISEL Academic Journal of Electronics, Telecommunications and Computers
Vol. 6 , n. 1 (2020) ID-6

Applications for a-Si:H TFTs: Modelling and Simulation

P. Lourenço[2,3], A. Fantoni[1,3], M. Fernandes[1,3], J. Costa[1,3], M. Vieira[1,2,3]
1. ISEL/ADEETC - Instituto Superior de Engenharia de Lisboa, Instituto Politécnico de Lisboa, Área Departamental de Engenharia Eletrónica e Telecomunicações e de Computadores, Rua Conselheiro Emídio Navarro, 1, 1959-007 Lisboa, Portugal;
2. Faculdade de Ciências e Tecnologia, FCT, Universidade Nova de Lisboa, Departamento de Engenharia Eletrotécnica, Campus da Caparica, 2829-516 Caparica, Portugal;
3. CTS-UNINOVA, Campus da Caparica, 2829-516 Caparica, Portugal.
plourenco@deetc.isel.ipl.pt afantoni@deetc.isel.ipl.pt mfernandes@deetc.isel.ipl.pt jcosta@deetc.isel.ipl.pt mv@deetc.isel.pt

Abstract - Hydrogenated amorphous silicon thin film transistors have been used as switching elements in liquid crystal displays and large area matrix addressed sensor arrays. Later, these devices have also been used as analogue active elements in organic light emitting diode displays. However, this technology suffers from bias induced meta-stability. This issue introduces both threshold voltage and subthreshold slope shifts over time when gate bias is applied. Such instabilities jeopardize long term performance of circuits that rely on these components. Nevertheless, hydrogenated amorphous silicon thin film transistors present an exponential transfer characteristic when operating on subthreshold region and their typical power consumption is under 1 µW. This low power characteristic makes these devices ideally suited for low power electronic design.

This work demonstrates, through transient analysis of a well-established simulation model for hydrogenated amorphous silicon, the viability of thin film transistors technology to perform both analogue and digital functions. Hence, these structures may be used in both application fields. To this end, two different sets of analyses have been conducted with hydrogenated amorphous silicon based thin film transistors. The first set considers a driving circuit for an active matrix of organic light emitting diodes, biased in a way to minimize the "memory effect" (increasing shift on threshold voltage) due to long term operation. The second set of analyses were conducted upon the implementation of complementary output universal gates, namely NOR/OR and XNOR/XOR elements.

Keywords: thin film transistors, hydrogenated amorphous silicon, AMOLED driving circuit, universal gates.

I. Introduction

The first thin film transistor (TFT) has been developed in Princeton, USA, at the RCA Laboratories (1962) and cadmium sulphide was the selected semiconductor for the active layer. This happened right after the first presentation, by Mohamed Atalla and Dawon Kahng, of the metal-oxide-semiconductor field effect transistor (MOSFET) at the Solid-State Device Conference, held at the Carnegie Mellon University, in 1960 [1]. Nevertheless, commercially successful TFTs were only obtained in the 1980s, when hydrogenated amorphous silicon (a-Si:H) was included as the active layer semiconductor [2].

A TFT is essentially a MOSFET (see Figure 1), only the semiconductor is deposited on an insulating substrate as a thin film layer for the former, as opposed to the bulk semiconductor body/substrate in conventional MOSFET. Moreover, bulk MOSFETs operate in the inversion mode and typical TFTs engage in the accumulation mode [3]. For comparison purposes, the semiconductor film thickness in TFTs ranges from 30-100 nm, though for single-crystal bulk silicon devices, the substrate depth usually is the silicon wafer thickness, spanning [4] from ~100 µm-1 mm.

Figure 1 illustrates, in a) a standard MOSFET, in b) the silicon-on-insulator (SOI) technology often used devices and, in c), the TFT structure. The resemblance is evident, namely between c) (TFT) and b) (partially depleted SOI), for both operate with a floating semiconductor channel (i. e. the channel material does not extend over the whole substrate width).

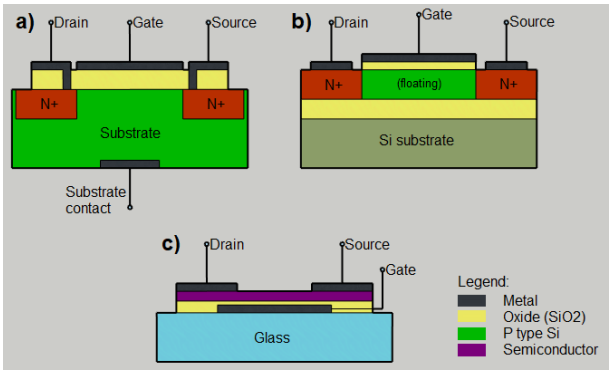

Figure 1 - SOI typical MOSFETs, a) and b), and TFT, c), structures.

Hence, TFTs possess low leakage and good device isolation, better latch-up immunity, protection against radiation, low parasitic capacitances, reduced substrate noise and their architecture design simplicity requires no doped drain and source regions [5].

a-Si:H TFTs main disadvantage is their low charge carriers' mobility. Amorphous semiconductors owe their low mobility to the transport of charge being dominated by thermally activated transport of localized charge carriers. Moreover, the mobility of carriers is directly related to the maximum current handling capacity and switching speed of the device. This may be concluded by comparing the I/V curves depicted on Figure 2 and Figure 3. Here, the simulated DC transfer curves of an off-the-shelf Si based MOSFET and an a-Si:H based TFT, obtained when considering identical drain currents, are presented.

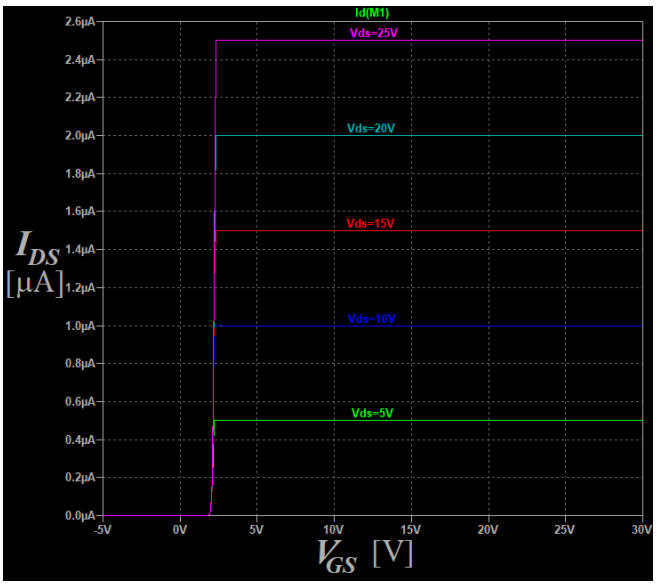

Figure 2 - I/V curves of an off-the-shelf MOSFET.

As may be observed, the a-Si:H TFT graphic denotes a less abrupt transition on the subthreshold linear region of the I/V curve. This is due to the lower charge carriers' mobility, which compromises the maximum driving current and switching capability for these devices. Nevertheless, using TFTs to drive application devices such as sensors and display arrays, where the required operating current and frequency are of some microamperes and a few kilohertz, this technology will be able to perform adequately.

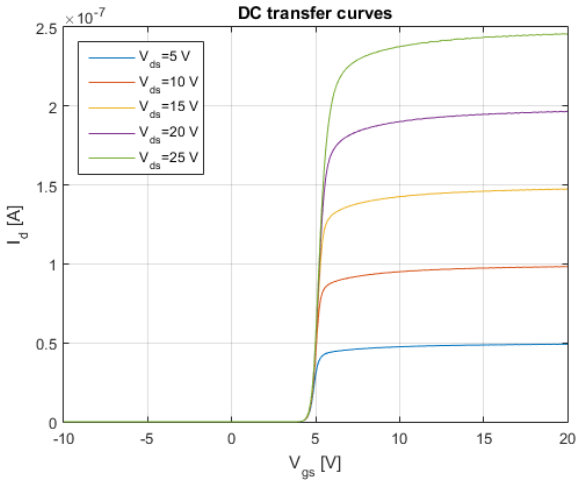

Figure 3 - I/V curve of an a-Si H based TFT for increasing Vds.

a-Si:H TFTs have been intensively used in driving liquid crystal displays (LCDs) [3]. The commercial success of these display arrays has proportionated the study and development of evermore efficient TFTs throughout a myriad of applications in multidisciplinary fields such as bioelectronics, optoelectronics and more. Contemporaneous useful application areas for these devices are [6]:

- Advanced large display arrays;
- Sensor arrays;
- RFID tags;
- Other disposable electronics.

In this article, the simulation of a-Si:H TFT devices has been conducted in the Automated Integrated Circuit Modelling Spice (AIM-SPICE) simulator [7], which has been configured with ASIA2, an a-Si:H TFT level 15 SPICE model [8]. This model consists on a set of equations and corresponding parameters that enable the analysis of the DC operating point, AC small signal, transient and steady state of a-Si:H based TFT devices. Namely in this model, the drain to source current is given by:

$$I_{ds} = I_{leakage} + I_{ab} \quad (1)$$

where,

$$I_{ab} = g_{ch} V_{dse} (1 + LAMBDA * V_{ds}) \quad (2)$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)} \quad (3)$$

$$g_{chi} = q n_s W \cdot MUBAND/L \quad (4)$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}} \quad (5)$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX} \left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA} \quad (6)$$

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \frac{V_{gfbe}}{V0} \frac{EPSI}{EPS}\right)^{\frac{2 \cdot V0}{V_e}} \quad (7)$$

$$n_{so} = N_c t_m \frac{V_e}{V0} exp\left(-\frac{DEF0}{V_{th}}\right) \quad (8)$$

$$N_c = 3.0 \cdot 10^{25}\ m^{-3} \quad (9)$$

$$V_e = \frac{2 \cdot V0 \cdot V_{tho}}{2 \cdot V0 - V_{tho}} \quad (10)$$

$$t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}} \quad (11)$$

$$V_{gfbe} = \frac{VMIN}{2}\left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right] \quad (12)$$

$$V_{gfb} = V_{gs} - VFB \quad (13)$$

$$V_{dse} = \frac{V_{ds}}{[1 + (V_{ds}/V_{sate})^M]^{1/M}} \quad (14)$$

$$V_{sate} = \alpha_{sat} V_{gte} \quad (15)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM) \quad (16)$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right] \quad (17)$$

$$V_{gt} = V_{gs} - V_T \quad (18)$$

$$V_T = VTO + KVT(TEMP - TNOM) \quad (19)$$

$$I_{leakage} = I_{hl} + I_{min} \quad (20)$$

$$I_{min} = SIGMA0 \cdot V_{ds} \quad (21)$$

$$I_{hl} = IOL\left[exp\left(\frac{V_{ds}}{VDSL}\right) - 1\right] exp\left(-\frac{V_{gs}}{VGSL}\right) exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right] \quad (22)$$

$$V_{aat} = VAA\ exp\left[\frac{EMU}{q \cdot GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right] \quad (23)$$

$$V_{th} = k_B\,.\,{}^{TEMP}/_{q} \quad (24)$$

$$V_{tho} = k_B\,.\,{}^{TNOM}/_{q} \quad (25)$$

In previous equations, all capitalized acronyms are parameters that, once acquired from the actual physical device, may be input into the model to better describe and to assure realistic analysis of the outcome from simulations. Table 1 presents these acronyms along with the used values in our simulations and a brief description of each parameter.

Table 1 - AIM-SPICE model ASIA2, level 15 parameters description.

ALPHASAT	Saturation modulation parameter	$\mathbf{0.6}$
CGDO	Gate-drain overlap capacitance per meter channel width	$0\ F/m$
CGSO	Gate-source overlap capacitance per meter channel width	$0\ F/m$
DEF0	Dark Fermi level position	$0.6\ eV$
DELTA	Transition width parameter	5
EL	Activation energy of the hole leakage current	$0.35\ eV$
EMU	Field effect mobility activation energy	$0.06\ eV$
EPS	Relative dielectric constant of substrate ($\varepsilon_r\ of\ SiO_2$)	3.9
EPSI	Relative dielectric constant of gate insulator ($\varepsilon_r\ of\ SiO_2$)	3.9
GAMMA	Power law mobility parameter	0.4
GMIN	Minimum density of deep states	$10^{23}\ m^{-3}eV^{-1}$
IOL	Zero bias leakage current	$3 \times 10^{-14}\ A$
KASAT	Temperature coefficient of ALPHASAT	$0.006\ 1/℃$
KVT	Threshold voltage temperature coefficient	-0.036 V/℃
LAMBDA	Output conductance parameter	$0.0008\ 1/V$
M	Knee shape parameter	2.5
MUBAND	Conduction band mobility	$0.001\ m^2/Vs$
RD	Drain resistance	$0\ \Omega$
RS	Source resistance	$0\ \Omega$
SIGMA0	Minimum leakage current parameter	$10^{-14}\ A$
TNOM	Temperature measurement parameter ($TEMP = 300\ °K$)	27 ℃
TOX	Thin-oxide thickness	$10^{-7}\ m$
V0	Characteristic voltage for deep states	$0.12\ V$
VAA	Characteristic voltage for field effect mobility (determined by tail states)	$7.5 \times 10^3\ V$
VDSL	Hole leakage current drain voltage parameter	$7\ V$
VFB	Flat band voltage	$-3\ V$
VGSL	Hole leakage current gate voltage parameter	$7\ V$
VMIN	Convergence parameter	$0.3\ V$
VT0	Zero-bias threshold voltage	$0\ V$

This model has three main categories of parameters, the geometrical and technological related, the localised and defect states related, and the simulation curves optimization related [9]. In the first category are included, the drain (RD) and source (RS) resistances, the overlap capacitances between gate and drain (CGDO), and gate and source (CGSO), the insulating oxide thickness (TOX), the dielectric permittivities of both substrate and insulator layers (EPS and EPSI, respectively) and the leakage current when at zero DC bias (IOL). In the simulations presented throughout this report, the AIM ASIA2 model default values were used for the first category of parameters:

- **CGDO**;
- **CGSO**;
- **RD**;
- **RS**;
- **TOX**;
- **EPS**;
- **EPSI**;
- **IOL**.

The second category of parameters takes into account the distribution of localized (deep and tail) states and impurities of the a-Si:H channel, which include the undisturbed by external influences (voltage or radiation) Fermi level position (DEF0), the minimum density of deep states (GMIN) and their characteristic voltage (V0). The values assumed in the simulations were (AIM ASIA2 model default values):

- **DEF0** $\mathbf{0.6\ V}$;
- **GMIN** $\mathbf{10^{23} m^{-3} eV^{-1}}$;
- **V0** $\mathbf{0.12\ V}$.

For the third category of parameters, these are mainly extracted from a physical device through a process included in AIM-SPICE software and by the experimental interpretation of the curves obtained by the analysis of a given device. The simulations performed in this report have used the default values present in the AIM ASIA2 model, except when otherwise specified.
These parameters include:

- $\boldsymbol{\alpha_{sat}}$: - The saturation modulation parameter is temperature dependent and defines at which point gate saturation voltage takes place within the above threshold region. Equation (16) relates the saturation modulation (ALPHASAT) and its temperature coefficient (KASAT), together with the difference between the nominal (TNOM) and the external environment (TEMP) temperatures of the device. Equations (17,18,19) incorporate the influence of the zero-bias threshold voltage (VT0) and its temperature dependence, with the corresponding coefficient (KVT), into temperature dependent threshold voltage (V_T) and, ultimately, into the effective gate voltage (V_{gte}). Here, VMIN is an algorithm convergence parameter and DELTA defines the amplitude of the forward subthreshold region, as the transition width parameter. Finally, equation (14) describes the effective drain source voltage (V_{dse}), where the sharpness of the knee

transition between the linear and saturation regions is given by M, the knee shape parameter.

- $\boldsymbol{V_{aat}}$: - The characteristic voltage for charge mobility in the field effect activated channel, which is temperature and tail states density dependent. Equation (23) relates this parameter with the characteristic voltage for charge mobility (VAA), affected by the influence of the gradient between the nominal (V_{tho}) and external (V_{th}) temperatures on the field effect mobility (characterized by the ratio between its field effect activation energy (EMU) and power law gate dependence (GAMMA) parameters).

The drain leakage current ($\boldsymbol{I_{leakage}}$) grows exponentially with the negative increase of gate-source voltage. According to [10], the current in the Poole-Frenkel region results from an accumulation of holes in the vicinity of the gate-drain overlap, which facilitates a conduction path in reverse direction. Equations (20, 21, 22) define this drain current by incorporating the influence of corresponding minimum current (SIGMA0), temperature and activation energy hole current (EL), and hole currents gate (VGSL), drain (VDSL) and zero-bias (IOL) voltages parameters.

The above- and sub-threshold drain current ($\boldsymbol{I_{ab}}$) considers previously referred equation (14), the effective drain source voltage (V_{dse}), a conductance parameter (g_{ch}) and an output conductance parameter (LAMBDA) that corresponds to the channel length modulation. The channel conductance (g_{ch}) depends on the intrinsic channel conductance (g_{chi}) and on the drain (RD), and source (RS) resistances. On its turn, the intrinsic channel conductance (g_{chi}) is influenced by the geometrical dimensions of the channel (W and L) and the mobility in the conduction band (MUBAND) affected by a parameter (n_s) that, ultimately, depends on the density of localized states in the channel (N_C).

II. Pixel Driving Circuit

Research on active matrix organic light emitting devices (AMOLEDs) technology for advanced displays has been an area of intense study. This technology is able to provide thin and lightweight devices with wide viewing angle, fast reaction times and operating at low power. One of the main constraints concerning AMOLEDs is their lifetime when on normal operation. Figure 4 shows the TFT modelled behavior of threshold voltage over time and with temperature, of an SiO2 gate insulated a-Si:H TFT, on an inverted staggered configuration [9].

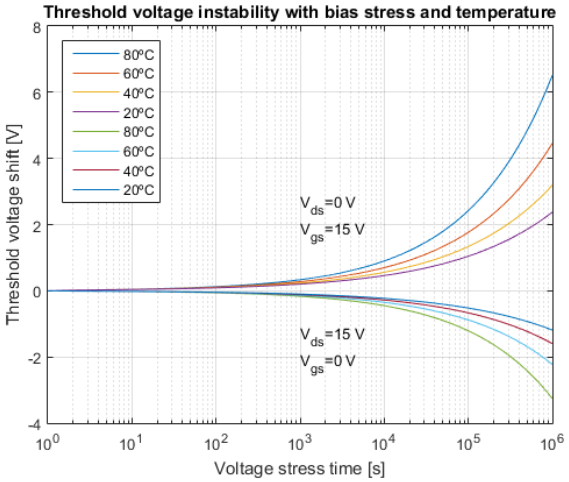

Figure 4 - TFT threshold voltage over time and with temperature.

One must keep in mind that Figure 4 depicts a steady state bias stress applied to the TFT's gate, drain and source, which is not the case when on normal AMOLED operation. When TFTs operate as such, their gate is pulsed with a very low duty-cycle (0.01% to 1%) which, consequently, results in much longer time periods of operation for a given threshold voltage shift. Moreover, the threshold voltage shifts with time predicted by Figure 4, are in a much smaller scale than the ones verified in OLEDs (0.7 V shift for a period of 3 hours at -10 V which is equivalent to the shift verified under identical forward biasing) [11].

Nevertheless, there have been reports stating that the driving scheme is a key element, when performance improving for these devices is intended. AMOLEDs can be driven either by a direct current (DC) or alternate current (AC) schemes. The former driving mode has been more extensively used than the latter, for it was initially considered one of the major advantages and features for these devices [12]. However, research on AC driving mode has also been conducted and promising results reporting an extended lifetime, have been published by several researchers. At the same time, it has been reported that a constant current driving mode achieves longer lifetimes than a constant voltage one [11].

In this work, a basic AC driving circuit is presented, and its operation is characterized through simulation. Specifically, this circuit operates as a pulse driving mode, combined with a reversed bias component to improve AMOLED lifetime. These two driving mode components should be able to assure better performance and accelerated recovery from

degradation. The basic pixel addressing circuit is depicted in Figure 5.

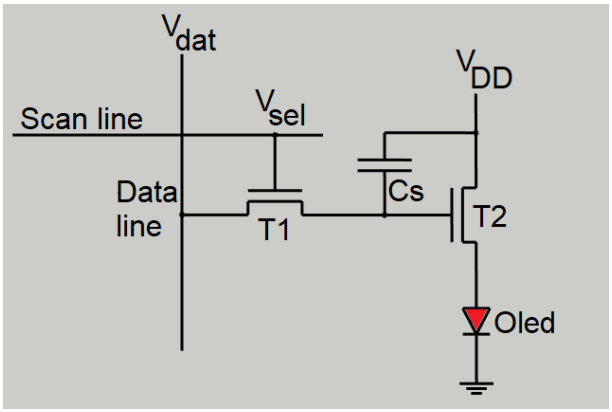

Figure 5 - Basic pixel driving circuit.

This circuit is essentially formed by four elements. Transistor T1, which is addressable through V_{sel} on Scan line, transistor T2 is a current source element, the OLED element and capacitor C_s. Current source behaviour-like is assured by biasing transistor T2 in saturation and this constant current drives the OLED element. The circuit operates as follows:

- Current source T2 is controlled by data voltage V_{dat}. When T1 is turned on through V_{sel}, V_{dat} is transferred to the gate of T2 and stored across C_s which assures that the OLED pixel current/brightness is kept almost unaltered until the next frame period.

The OLED pixel structure can be modelled by a diode in parallel with a capacitor, as represented in Figure 6:

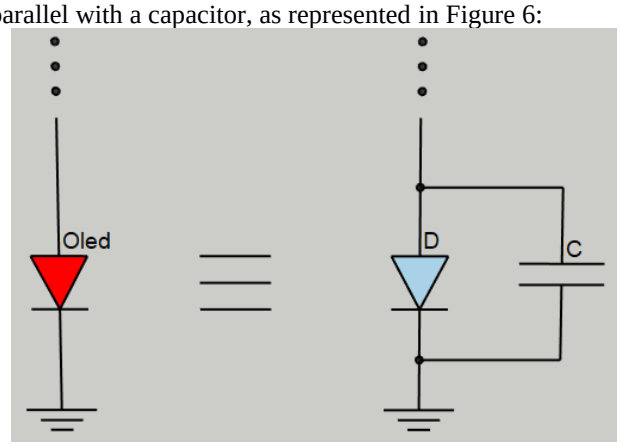

Figure 6 - OLED pixel equivalent circuit.

Capacitance of an OLED small organic molecule and its associated polymeric diode depends on the area of the element and is approximately [12] 25 nF.cm^{-2}. Thus, considering the assumed dimensions of 110 x 330 µm for one element of the pixel structure, the aperture capacitance will be ~9 pF.

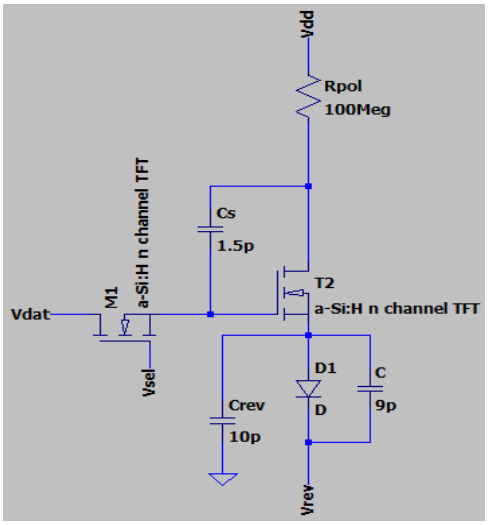

Figure 7 - OLED driving circuit.

To compensate the influence of this capacitance and provide the AC operating mode capability, an extra capacitor, C_{rev}=10 pF, and a reversing polarization, V_{rev}, are included. For previously mentioned and still not defined component Cs, 1.5 pF has been the selected value, resulting on the circuit presented in Figure 7, which has been designed with the help of LTspiceXVII, a SPICE based physical simulator [13].

A. Circuit operation

The purpose of this work is to demonstrate through simulation that an AMOLED might be AC driven by a-Si:H thin film transistors (TFTs). To this end, the AIM-SPICE analogic circuit simulator [7] with a precise a-Si:H TFT model has been utilized, after netlist importing from LTspiceXVII.

Considering the circuit of Figure 7, where M1 and T2 are a-Si:H TFTs with widths and lengths of 33x11 µm. If the magnitude and duration of V_{rev} pulse are large and long enough, the OLED pixel is reversely biased and its current is maintained, except for the duration of V_{rev} pulse when the current through the structure is decreased almost to zero. Thus, AC mode operation is guaranteed and simulation resulting waveforms are shown in Figure 8-10.

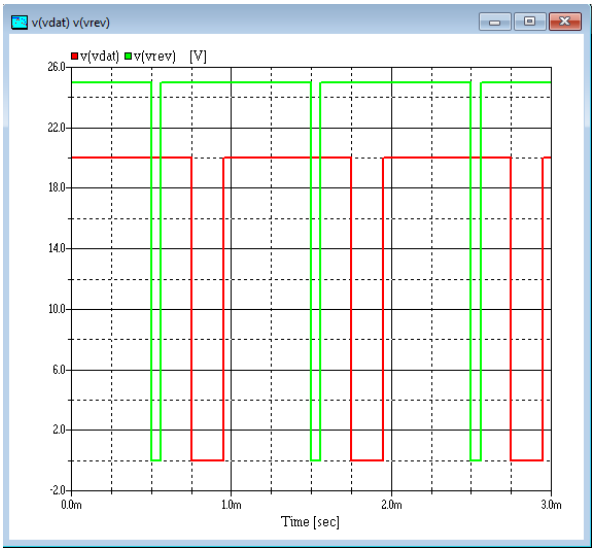

Figure 8 - Vdat and Vrev waveforms.

V_{dat} is a train of *200 µs* pulses with *1 ms* period that emulates incoming data line. V_{rev} and V_{sel} are time synchronized pulses, both with *1 ms* period and duration *60 µs*; the former assures reverse/forward biasing to T2 and the latter mimics pixel addressing through the scan line.

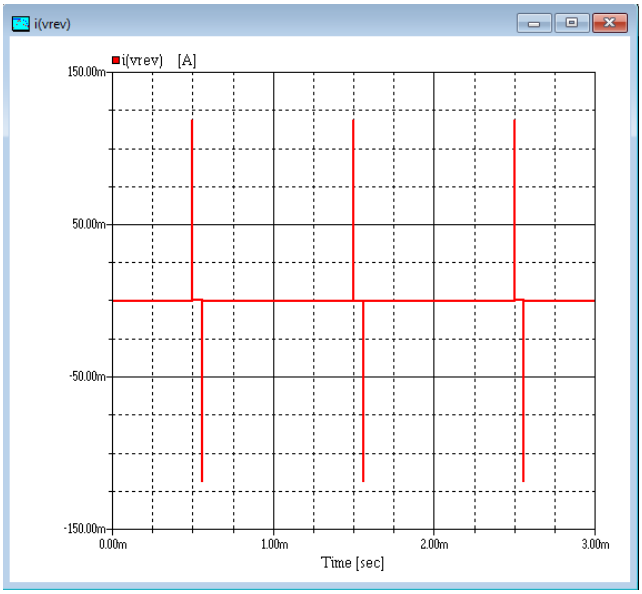

Figure 9 - Current through Vrev (confirming AC mode operation).

Figure 9 shows the current that flows through the voltage supply V_{rev}. This bias is connected to the OLED pixel "cathode" end, thus current flowing through V_{rev} is the same current going through the OLED pixel. Observing the graphic of Figure 9, one is able to notice that the mean current value going through the OLED pixel over time is zero. This confirms OLED pixel AC mode operation which, combined with a reversed-bias voltage, is expected to improve OLED lifetime [11]. Transient response at the diode's anode (V_{OLED}) is depicted in Figure 10. Here, it is noticeable the reverse bias operation and that voltage amplitude remains almost unaltered until the end of the frame period, thus providing stability to OLED luminance.

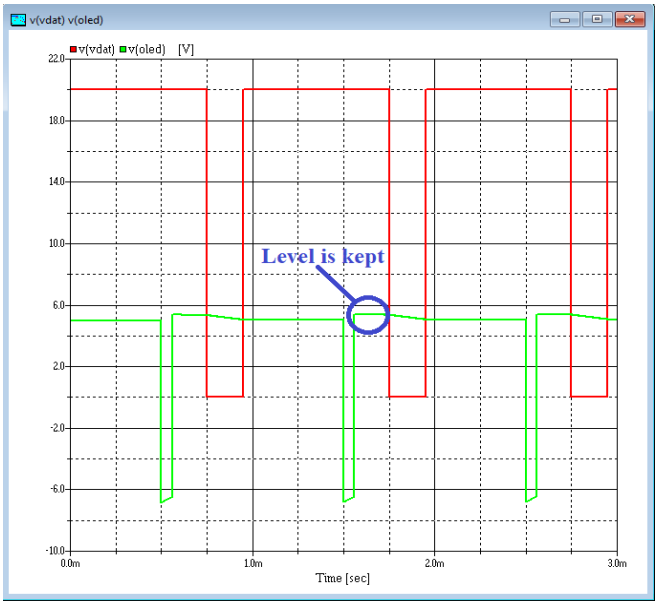

Figure 10 – V_{OLED} waveform (voltage level is maintained throughout frame period).

B. Four OLEDs AC mode driving

This work refers to a basic driving circuit for AMOLEDs, thus the next step considered simulating an 1x4 matrix of OLEDs. The resulting four-pixel circuit is merely a repetition of the unit circuit and all characteristics and principles of operation remained the same. Figure 11 shows the 4-pixel driving circuit designed with the help of LTspiceXVII.

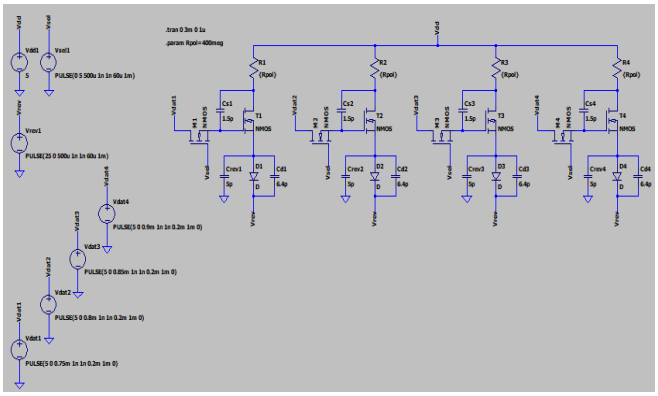

Figure 11 - 1 x 4 AMOLED driving circuit.

Next, a similar procedure as previously performed has been followed. Namely, exporting generated netlist to AIM-SPICE, transistors M1-M4 and T1-T4 have been configured with ASIA2, an a-Si:H TFT level 15 SPICE model, and correspondent widths and lengths, and transient analysis has been performed. It is worth mentioning that, in this circuit, V_{dat1} through V_{dat4} are each delayed by *50 µs* to emulate different timings on the data line for each pixel. The resulting waveforms at the "anode" end of each OLED are presented in Figure 12.

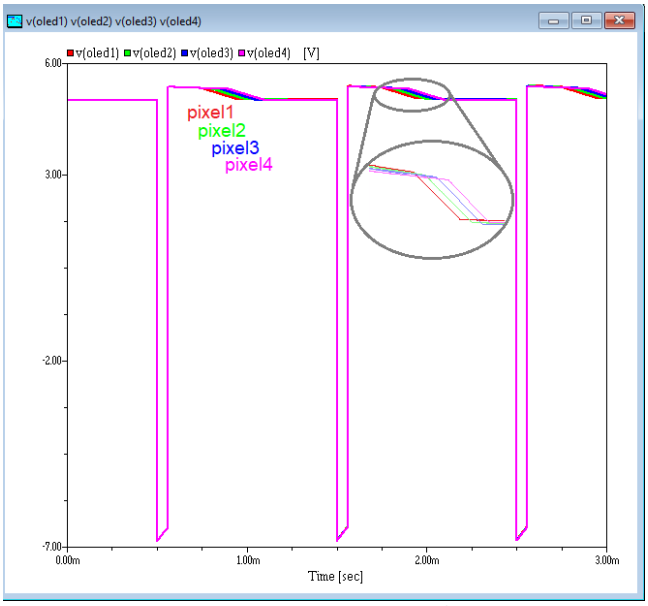

Figure 12 - Pixel1 to pixel4 waveforms.

Once more, one can observe that V_{OLED} amplitude is maintained almost constant for the remaining of the frame period after reverse biasing is applied, assuring insignificant decrease on AMOLED pixels luminance.

C. Digital elementary circuits

Any logic gate, thus any logical function, can be reproduced by a number of universal logic gates [5]. These universal elements are either NOR or NAND gates. Hence, any

technology able to fulfil the logical requirements of one of these universal gates, ultimately is a technology capable of reproducing all logical functions. TFTs fabricated upon a-Si:H based technology, may also be associated to reproduce the logical functionality of these universal logic gates.

In this work we will be presenting first, an a-Si:H based TFT association that performs as a logic NOR/OR gate, followed by another TFT circuit which logical behavior is of an XNOR/XOR gate. Both these circuits were designed and simulated as mentioned before in previous section. Namely, circuits were designed with the help of LTspiceXVII [13], the generated netlist was exported to AIM-SPICE, all TFTs have been configured with ASIA2, an a-Si:H TFT level 15 SPICE model [8], and considering *23 µm* and *400 µm* for each device's length and width, respectively.

Because logic operation was the intended functionality, it is necessary that all TFTs operate in saturation. This requires the I-V curve knowledge for optimal operation point determination. Referring to Figure 3, where it is shown the a-Si:H TFT drain to source current, as the gate to source voltage is iterated from -10 V to 30 V with increasing values of drain to source voltage, one may consider that saturation occurs for $V_{gs}>10$ *V*, for all simulated values of V_{ds}.

Then, by using LTspiceXVII, a NOR/OR gate has been designed. This circuit is depicted in Figure 13, where V_a and V_b, and *Out* represent the logic gate inputs and output, respectively. Inputs rise and fall times were assumed to be *100 µs*, and capacitors C_1 and C_2 have been included to smoothen OR and NOR switching fluctuations. These capacitances were set empirically through a series of trial and error iterating attempts.

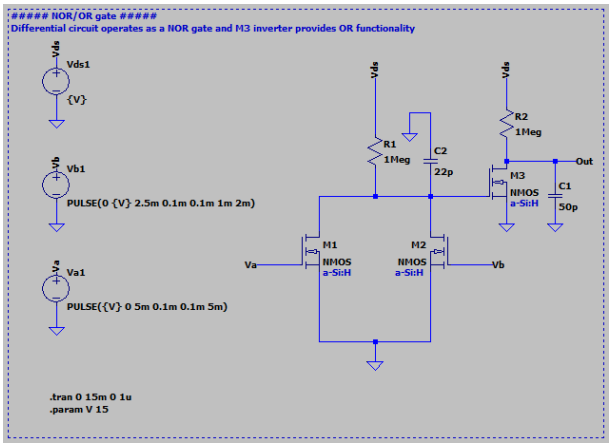

Figure 13 - NOR/OR gate circuit implementation.

To verify gate's functionality, inputs V_a and V_b were set according to Figure 14 (two square waves with different periods), with maximal amplitude of 15 V and raise/fall times of *100 µs*.

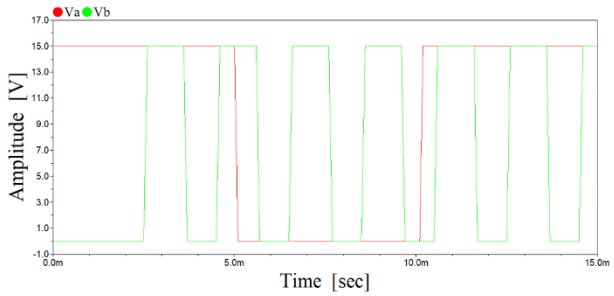

Figure 14 - Va and Vb inputs.

Once more, transient analysis was executed for a time period of *15 ms* and the results obtained are presented in Figure 15 and Figure 16.

Figure 15 presents the voltage levels obtained at the gate node of M3 (see Figure 13), which is the outcome result of applying the conditions depicted in Figure 14 at V_a and V_b input nodes. Similarly, Figure 16 shows the OR functionality that was obtained at the drain node of M3 (see Figure 13) under the same input conditions.

Next, one more logic gate has been designed, simulated and analyzed. This time the evaluated element was a XOR/XNOR gate and the correspondent circuit implemented in AIM-SPICE is depicted in Figure 17:

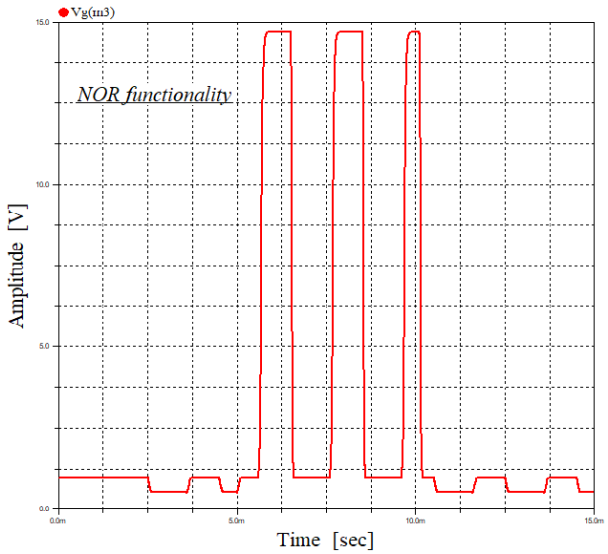

Figure 15 - NOR waveform.

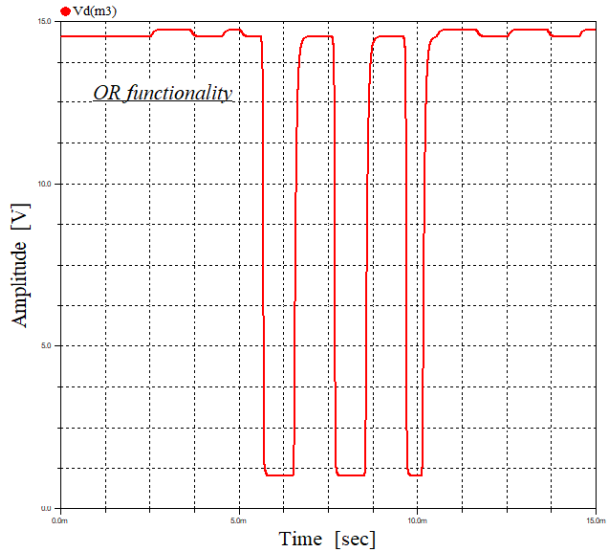

Figure 16 - OR waveform.

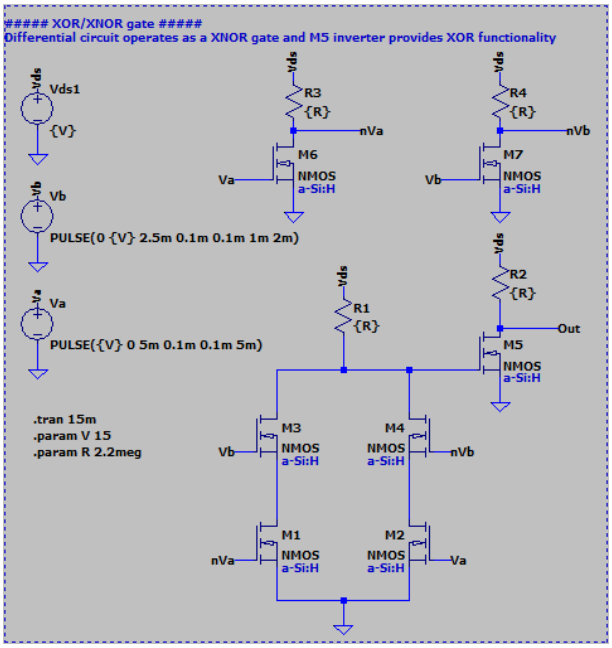

Figure 17 - XNOR/XOR gate circuit implementation.

The design of a XOR/XNOR gate requires both inverted and non-inverted inputs, hence the inclusion of inverters M6 and M7 on the above circuit schematic. Also, inverter M5 provides the complementary output functionality.

The same procedure, as before with the NOR/OR gate, has been followed. Netlist from LTspiceXVII has been imported into AIM-SPICE and all TFTs have been configured with ASIA2, a level 15 a-Si:H model. At the input nodes, V_a and *Vb*, were applied the same periodic square waves depicted in Figure 14. Again, transient analysis was conducted for a time duration of *15 ms* and the results obtained are presented in Figure 18 for XNOR logic operation and in Figure 19 for XOR functionality.

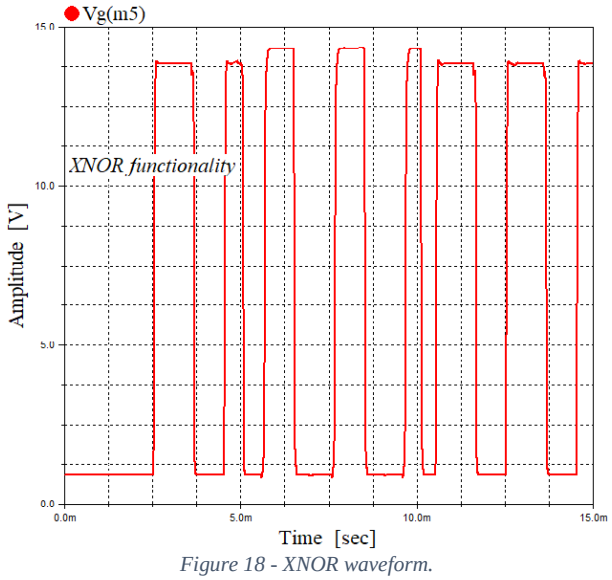

Figure 18 - XNOR waveform.

XOR response shows better waveform stability and wider voltage differentiation between high- and low-level states, than XNOR response waveform. Nevertheless, the agreement between the presented waveforms and XNOR/XOR truth tables is evident, hence one may say that a-Si:H based TFTs are able to perform as a building block of more complex digital circuitry.

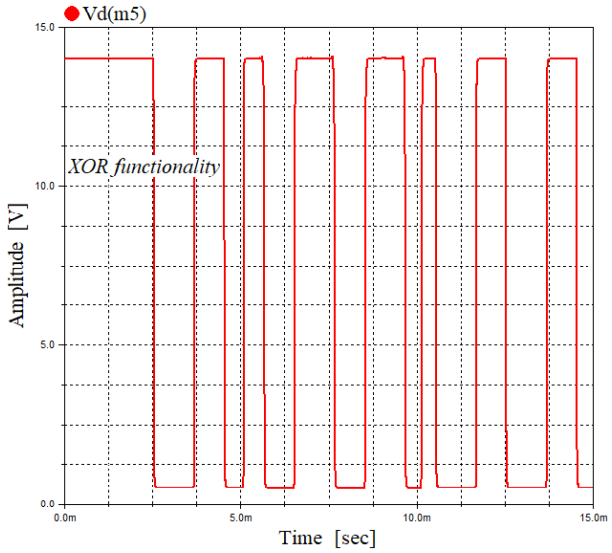

Figure 19 - XOR waveform.

TFTs based on a-Si:H technology may operate as the building blocks of digital and analogic circuitry, but their low mobility presents serious constraints for applications requiring fast operation. Once the frequency of operation starts increasing, these devices are not able to respond adequately, giving way to a drastic decrease in performance. To illustrate this behavior, the circuit implementation depicted in Figure 17 has been simulated with higher operating frequencies and the obtained results are presented next.

Previous waveforms depicted on Figure 18 and Figure 19 correspond to a maximum pulse frequency of *500 Hz* at the input nodes. Figure 21 shows the waveforms obtained at the gate (XNOR) and drain (XOR) of m5 TFT, for an increase of an order of magnitude in the maximum operating frequency (*5 kHz*) performed at the V_b input, as presented in Figure 20.

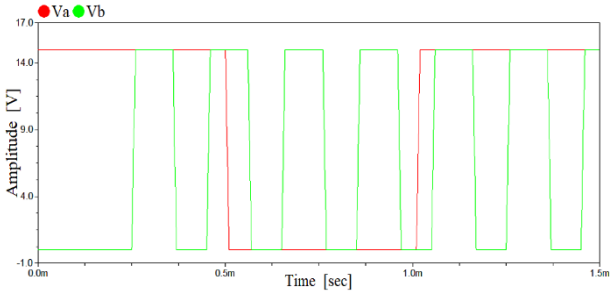

Figure 20 - Va and Vb (maxim frequency = 5 kHz) inputs.

It is evident the difference in performance between Figure 18 and Figure 19 and the correspondent waveforms obtained in Figure 21. The frequency increase induced a degraded response of the circuit, namely at the XNOR functionality.

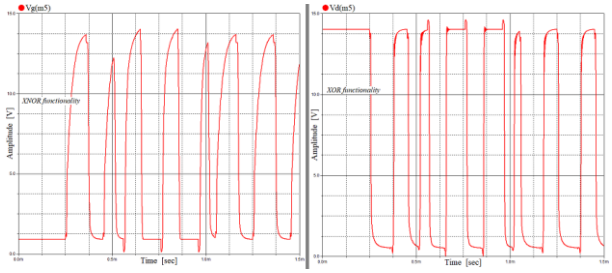

Figure 21 - XNOR and XOR waveforms at 5 kHZ maximum operating frequency.

Maximum operating frequency was further increased to *10 kHz*, resulting in the waveforms depicted in Figure 22. Again, there is a difference in performance when XNOR and XOR functionalities are compared. Although XOR functionality is still clearly present, XNOR waveforms denote lower response performance which limits the intended functionality. This distinction between XNOR and XOR performances may be minimized by decreasing the ohmic value of R1, nevertheless this happens at the expense of a reduction on the performance of XOR functionality (ringing increase after low-high edge transition).

Looking at equations (1), (2), (3) and (4), one may see that the current I_{ab} is directly related to the channel conductance g_{ch} which, on its turn, depends directly on the width (W) and inversely on the length (L) of the channel. All the other influential parameters are either intrinsic of the technology or dependent of the manufacturing process. Typically, the channel length (L) is set as a constant for a given fabrication process, which leaves only the width (W) of the a-Si:H channel as a designing variable, together with the gate and drain bias voltages, to try to improve the TFT device performance.

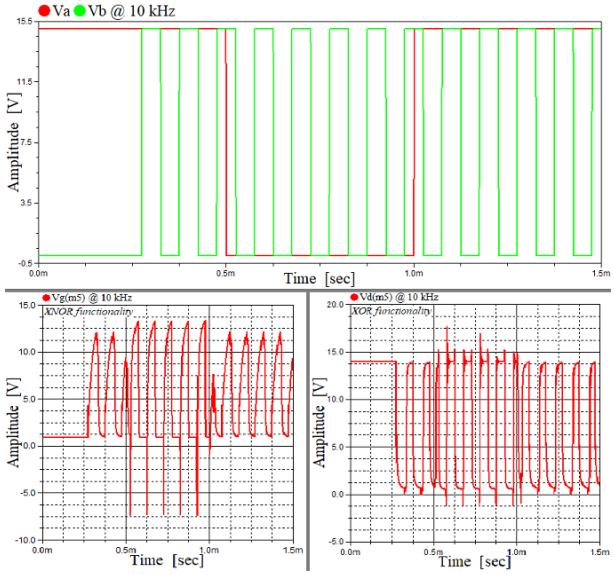

Figure 22 - Va and Vb inputs, and XNOR/XOR waveforms at the maximum operating frequency of 10 kHz.

As an end note for this section, we would like to add that previous circuits (NOR/OR and XNOR/XOR) are able to provide, within the frequency limits previously mentioned, complementary output functionality for they implement both logic gate and its logical complement functions.

D. Fanout

The fanout definition refers to the number of load gates, of identical design, that might be connected to the output of a driver gate. As a-Si:H TFT based logic gates require essentially no quiescent current to drive similar devices, in terms of static DC characteristics, the number of connected gates to one output is virtually infinite. However, when taking into consideration the propagation delay time, associated to logic level switching across a network of connected devices, such is not true anymore.

When a driver gate changes states, it does so by charging/discharging the load capacitance. This functionality may be modelled by a current source (the driver) connected to a capacitive load (the connected device), as depicted in Figure 23a). As more devices are connected to the gate driver, as shown in Figure 23b), the load capacitance that must be charged/discharged increases. This places a limit on the number of connected gates to the same driver device, for the RC time constant of the circuit increases, which extends in time the charging/discharging cycles.

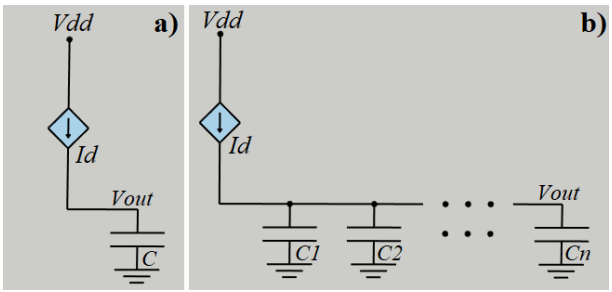

Figure 23 - Capacitive load with a) single and with b) several connected devices.

The output voltage, V_{out}, is then given by [14]:

$$V_{out} = \frac{1}{C}\int_{-\infty}^{t} I_d\, dt = \frac{I_d t}{C} \tag{26}$$

Load capacitance C is the summation of all (n) individual input gate capacitances and the driving current relates directly to the driver conductance. Hence, we may consider the switching time as:

$$t = \frac{n(W \times L)_{load}}{\left(\frac{W}{L}\right)_{driver}} \tag{27}$$

This is so because the driving device current is controlled by the ratio, W/L (see equation (28), where μ_n is the mobility when at saturation, C_{ox} is the capacitance created by the insulator layer (SiO_2), V_{gs} is the gate to source voltage and V_t is the threshold voltage), and the loading gate capacitance (see equation (29)) is directly related to the cross section, $(W*L)_{load}$, of each connected device [15].

$$I_{drive} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right)^2 \tag{28}$$

$$C_{ox} = \frac{\varepsilon_{ox} WL}{TOX} \tag{29}$$

III. CONCLUSIONS

AMOLEDs operating in a constant current driving mode have longer lifetimes than when operating in a constant voltage driving mode. By applying a reverse bias component together with current pulse driving, enabling OLED pixels to operate in AC driving mode, the expectations are to compensate for TFT's threshold voltage deviation when on prolonged operation and, consequently, improve the lifetime of these devices.

In the Pixel Driving Circuit section of this article, it has been demonstrated through analysis and simulations that AMOLED devices may be AC driven by a-Si:H TFTs, and consequently lengthen their lifetimes. Moreover, this may be achieved without compromising any OLED's luminance for their voltage level remains almost constant after selection and for the rest of the frame period.

Next followed the Digital elementary circuits section where it has been explored the feasibility of developing digital

circuitry with a-Si:H based TFTs as the building blocks. Any logic gate behavior may be reproduced by a number of universal gates. NAND and NOR gates are universal gates for they can implement any Boolean function by themselves (i. e. without the need of any other gate type). Hence, any technology able to implement one of these universal gates would be capable of reproducing any digital function. In this latter section, it has been demonstrated the capability of a-Si:H TFT technology to design complex digital circuits for it has been implemented an OR and a XOR complementary output gates. Both gates logical behavior has successfully been validated through simulation and transient analysis. However, these circuits performance is highly affected by the operating frequency. The low charge mobility presented by these devices leads to poor performance for switching frequencies above 10 kHz.

Moreover, we have included some background information about the Fanout associated to a-Si:H TFTs and both perspectives, static DC and dynamic, have been approached. We have also derived the equations to obtain the maximum number of connected gates to a given TFT driving device.

Acknowledgements

This work has been supported by Portuguese national funds provided by FCT – Fundação para a Ciência e a Tecnologia through grant SFRH/BD/144833/2019.

References

[1] D. Kahng, "A historical perspective on the development of MOS transistors and related devices," *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 655–657, Jul. 1976, doi: 10.1109/T-ED.1976.18468.

[2] P. G. Le Comber, W. E. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electron. Lett.*, vol. 15, no. 6, pp. 179–181, 1979, doi: 10.1049/el:19790126.

[3] A. Sharma, C. Madhu, and J. Singh, "Performance Evaluation of Thin Film Transistors: History, Technology Development and Comparison: A Review," *Int. J. Comput. Appl.*, vol. 89, no. 15, pp. 36–40, 2014, doi: 10.5120/15710-4603.

[4] M. R. Marks, Z. Hassan, and K. Y. Cheong, "Ultrathin Wafer Pre-Assembly and Assembly Process Technologies: A Review," *Crit. Rev. Solid State Mater. Sci.*, vol. 40, no. 5, pp. 251–290, 2015, doi: 10.1080/10408436.2014.992585.

[5] T. D. Takayasu Sakurai, Akira Matsuzawa, *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications - Takayasu Sakurai, Akira Matsuzawa, Takakuni Douseki - Google Books*.

[6] R. Street, *Technology and Applications of Amorphous Silicon*, vol. 37. Berlin, Heidelberg: Springer Berlin Heidelberg, 2000.

[7] "AIM SPICE." http://www.aimspice.com/ (accessed Jan. 24, 2020).

[8] "AIM-Spice Reference Manual." http://homepages rpi.edu/~sawyes/AIMSPICE_TutorialManual.pdf (accessed Jan. 24, 2020).

[9] H. Aoki, "Dynamic characterization of a-Si TFT-LCD pixels," *IEEE Trans. Electron Devices*, vol. 43, no. 1, pp. 31–39, 1996, doi: 10.1109/16.477590.

[10] L. Zhu, "Modeling of a-Si : H TFT I-V Characteristics in the Forward Subthreshold Operation," *Current*, 2005.

[11] D. Zou, M. Yahiro, and T. Tsutsui, "Improvement of current-voltage characteristics in organic light emitting diodes by application of reversed-bias voltage," *Japanese J. Appl. Physics, Part 2 Lett.*, vol. 37, no. 11 SUPPL. B, pp. 9–12, 1998, doi: 10.1143/jjap.37.l1406.

[12] S. Yujuan, Z. Yi, C. Xinfa, and L. Shiyong, "A Simple and Effective ac Pixel Driving Circuit For Active Matrix OLED," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1137–1140, 2003.

[13] "LT Spice XVII." http://ltwiki.org/LTspiceHelpXVII/LTspiceHelp/html/LT_spice_overview.htm (accessed Jan. 24, 2020).

[14] A. Agarwal and J. H. Lang, *Foundations of Analog and Digital Electronic Circuits*. Elsevier Inc., 2005.

[15] S. M. Venugopal, "Flexible active matrix displays and integrated amorphous silicon source drivers," 2007.