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Website: Kjar.spu.edu.iq | Email: kjar@spu.edu.iq

MSVPWM Based-SAPF For Harmonic Mitigation in The Distribution Network Under Unbalanced Condition

Haider Muhamad Husen
Electrical Department
Kalar Technical Institute
Sulaimani Polytechnic University
Kalar, Iraq
haider.husen@spu.edu.iq

Salar Ahmed Qadir
Electrical Department
Kalar Technical Institute
Sulaimani Polytechnic University
Kalar, Iraq
salar.qadir@spu.edu.iq

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ABSTRACT

Unbalanced input source voltages generate extra current harmonics in addition to non-linear loads which distorts the power quality in the entire power systems. Three-phase multi-level neutral point clamped (NPC) converter based shunt active harmonic filter (SAHF) are used as a solution to overcome problems due to current harmonics. In this work, synchronous reference frame (d-q) algorithm is selected to detect the harmonic current components, Proportional-integral (PI) controller is utilized to ameliorate the storage of energy in the dc-link capacitor and the multilevel space vector pulse width modulation (MSVPWM) strategy determines the switching pulses of NPC inverter. Under balanced input supply voltages condition, the proposed MSVPWM achieved a mitigation of source current THD of 3.58 % as compared to 28.57 % prior to compensation on non-linear load. Furthermore, the MSVPWM technique was compared with and without compensation under unbalanced input source voltages and the results shows that the proposed method achieved reduction in source current THD of 3.96 % as compared to 29.76 % after and before compensation respectively. The proposed MSVPWM based-SAPF model was also compared with conventional SVPWM under balanced and unbalanced input supply voltages conditions. The results show that MSVPWM performed better than CSVPWM. The simulated results obtained by MATLAB/SIMULINK power system environment. All the results for the presented work are within IEEE-519 harmonics standard with non-linear loads under balanced and unbalanced voltages condition.

1. INTRODUCTION

Power quality is fundamentally the criterion of the three-phase source voltages. Imbalanced three-phase supply voltage in the distribution power system network is one of the disturbances that attenuate the power system quality [1, 2, and 3]. When the amplitude of three-phase voltages are unsymmetrical and are not exactly in (120°)phase shift, then the three-phase voltages is called imbalanced [1, 4].Total harmonic distortion (THD) in the distribution network increases due to disturbed three-phase power system. Consequently, polluted the power quality of supply [5].The vulnerability of electrical equipment with automated processing industry in low power quality drives to significant economic damages [6].To remove the harmonics of source line current, the passive power filter were used. However, the conventional passive L-C power filter have the drawback are bulkiness, fixed compensation and generates frequency resonance problems with other elements. As a result, the harmonic distortion in the source line current increased [7, 8, and 9]. In consequence of advances in power electronics devices, shunt active harmonic filter for harmonics repression in exporter harmonic current presented on the transmission line at a closest point to non-linear loads are developed [10].The techniques employed to extract the reference signal currents, strategies for generation the switching gate signals, inverter topologies and controller selected for dc-bus reference voltage determine the efficiency of SAPF [4]. Among the various techniques, to extract the current harmonics, SRF algorithm widely used for reference currents signal generation. Consequently, to its directness, accuracy and offer best stability when compared to other techniques [11].Conventional SVPWM is prominent as less harmonic distortion and higher dc-voltage utilization [12]. Traditional space vector pulse width modulation (TSVPWM) utilize symmetrical time of zero vector is better-known to create fewer harmonic than Carrier-Based PWM (CBPWM) [13]. Three-phase multi-level diode clamped converter (DCC) is renowned for digital controller implementation and reduced harmonics. Switching pulses signal of VSI are generating by three-level SVPWM technique for better output voltage level [14].This paper concentrated on the source current harmonics mitigation in power system distribution network. After explore and evaluation different types of switching sequences technique in harmonics reduction. Consequently, a three-level SVPWM (MSVPWM) method is presented for the suppression of supply current harmonics in power network. The performance of the evolution model with balanced and unbalanced power supply voltages condition is compared for CSVPWM based SAPF and three-level SVPWM based SAPF. The simulation results shown the efficiency of the proposed multi-level SVPWM based SAPF in reduced of source current harmonics.

2. SHUNT ACTIVE HARMONICFILTER COMPENSATOR

As a result of non-linear loads, both reactive power and harmonic currents contaminating the power supply network. To overcome this power quality issues, a SAPF is employed to inject an appropriate currents into the power distribution system at a point of line named as point of common coupling to compensate the current harmonics and reactive power, thereby SAPF compensator provided unity power factor. As demonstrated in Fig. 1. A typical structure of the SAPF connected to main voltage supply which consist of three-level voltage source inverter (VSI)with dc-bus capacitor acts as current controlled selected neutral point clamped (NPC) inverter, reference currents signal generation employed synchronous reference frame (SRF)algorithm and multilevel (MSVPWM) technique implemented for switching signal generation [15].

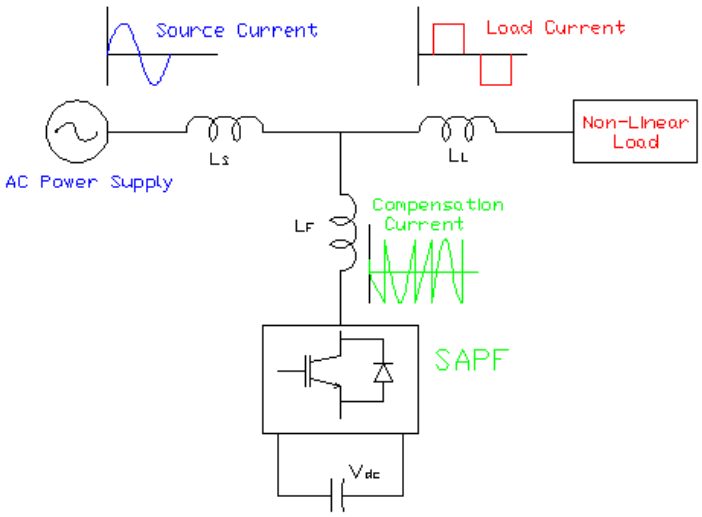


Figure 1: SAPF connected to PCC

2.1 Topology of Neutral Point Clamped Converter

An insulated gate bipolar transistor based three phase multi-level neutral point clamped inverter is illustrated in Fig.2, where one leg comprises of four power electronic switches (IGBT) shunted with ordinary freewheeling diodes. Two capacitors (C_1 and C_2) are employed to supply neutral point (zero voltage) at center between them. To clamp the inner two switches (S_2 and S_3) of single leg to half level ($V_{dc}/2$) of dc-reference voltage, the two diodes (D_1 and D_2) link-up to neutral point and accordingly well-known diode clamping inverter [16].

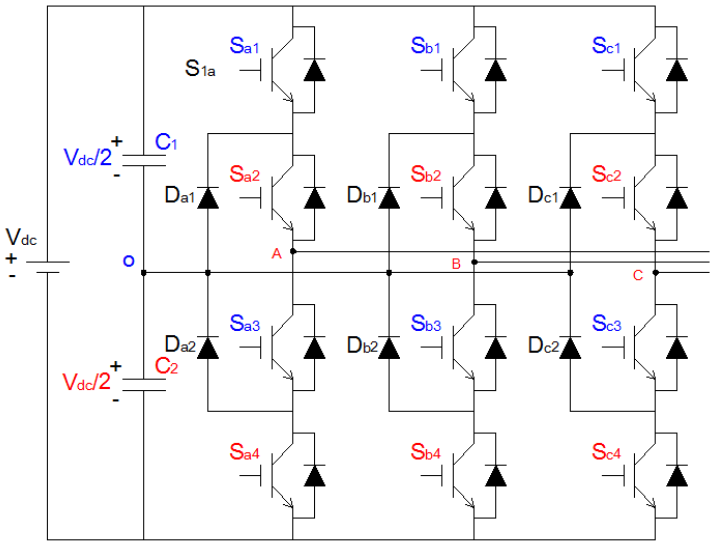


Figure 2: Three-level NPC inverter

Switching states of phase leg in three phase multi-level diode clamping inverter is illustrated in Table 1. When switching status is positive, it shows that the switches (S_1 and S_2) are linked to positive terminal of dc-link voltage and pole voltage is (V_{AO}), which indicates the pole voltage is ($+V_{dc}/2$). Whereas the switching status is negative, it exhibit that the switches (S_3 and S_4) are joined to negative side of dc-link

voltage, which denotes the pole voltage (V_{AO}) is ($-V_{dc}/2$). While the switching status is zero, display that the switches (S_2 and S_3) are switched ON. Therefore, the pole voltage (V_{AO}) is zero voltage (0) through one of the clamping diodes (D_1 and D_2) according to the path of load current.

Table 1: Switching Status for phase leg of multi-level diode clamping inverter

Switching Status	S_1	S_2	S_3	S_4	Pole Voltage
Positive	Active	Active	Inactive	Inactive	$+V_{dc}/2$
Zero	Inactive	Active	Active	Inactive	0
Negative	Inactive	Inactive	Active	Active	$-V_{dc}/2$

2.2 Synchronous Rotating Reference Frame (D-Q) Theory

To extract the reference current signals ($i_{abc-ref}\ stationary\ reference\ frame$) from the load currents, synchronous rotating frame (d-q) theory is applied. In SRF algorithm the load currents in three-phase stationary reference frame ($i_{Labc}\ stationary\ reference\ frame$)is converted into stationary two-phase ($i_{L\alpha\beta}\ stationary\ reference\ frame$)by utilized Clarke transformation as shown in equation (1)[17]

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

By exploited synchronous rotating frame($dq\ reference\ frame$), expression of load currents is given by equation (2)

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (2)$$

The synchronous angular position of the phase voltage is represented by(θ).As a result of non-linear load, the load currents in SRF technique (d-q components) are distorted by harmonic currents. Therefore, the load currents become as in equation (3)

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \bar{i}_{Ld} + \tilde{i}_{Ld} \\ \bar{i}_{Lq} + \tilde{i}_{Lq} \end{bmatrix} \quad (3)$$

Constituents of load currents are direct current (dc) and alternating current (ac), where represents fundamental and distorted respectively in d-q reference frame. Consequently, the alternating current (ac) components of d-q reference frame after eliminated from distorted load currents by using low pass filter (LPF)are converted to stationary two-phase($i_{\alpha\beta}\ stationary\ reference\ frame$)as in equation (4)

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}^{-1} \begin{bmatrix} \tilde{i}_{Ld} \\ \tilde{i}_{Lq} \end{bmatrix} \quad (4)$$

Thus, reference harmonic signals in stationary two-phase ($i_{\alpha\beta-ref}\ stationary\ reference\ frame$)are generated as in equation (5)

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} \tilde{i}_{Ld} \\ \tilde{i}_{Lq} \end{bmatrix} \quad (5)$$

Consequently, stationary two phase reference frame ($i_{\alpha\beta-ref}\ stationary\ reference\ frame$)is transformed to three-phase ($i_{abc-ref}\ stationary\ reference\ frame$)by utilized inverse matrix of Clarke transformation and thereby will be employed to generation of reference signal currents as in equation (6)

$$\begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} \quad (6)$$

2.3 SVPWM With Various Levels For SAPF

2.3.1Two-Level SVPWM Algorithm

A three phase two level voltage supply inverter which dedicates vectors as a reference voltage by employed a specific switching sequences of the six electronic switches it is called SVPWM control technique, where creates a fewer harmonics in source currents. Furthermore, a SVPWM utilize source voltage more efficient than conventional PWM. With a view to provides the reference voltage approach to the rotating flux, the SVPWM algorithm employed eight arranges of various switch modes of three phase two level voltage supply bridge-inverter, which includes two zero voltage vectors (V_0 and V_7) and six active voltage vectors (V_1,V_2,V_3,V_4,V_5,V_6) by used Clarke transformation to convert stationary three phases voltage ($V_{abc}\ stationary\ reference\ voltage$) to stationary two phase ($V_{\alpha\beta}\ stationary\ reference\ voltage$).As depicted in Fig. 3.a, the hexagonal of space vectors is created by two zero vectors and six active vectors as symbolized by V_0(000),V_1(100),V_2(110),V_3(010),V_4(011)V_5(001),V_6(101),V_7(111). The spatial plane ($\alpha\beta\ reference\ frame$)divided into six sectors (I-VI) by six active vectors with angle (60°)between the two nearest active vectors.

To approximate the vector of reference voltage to the rotating flux of three phase induction machines, the equations (7-8) are applied to constituted reference voltage vector (V_{ref}) by voltage vector (V_1) and voltage vector (V_2) in sector-I as clarified by Fig. 3.b.

$$T_z\overrightarrow{V_{ref}} = T_1\overrightarrow{V_1} + T_2\overrightarrow{V_2} \quad (7)$$

$$T_z = T_1 + T_2 + T_0 \quad (8)$$

Where (T_z) is sample time of SVPWM, time period of (V_1 and V_2) are represented by (T_1 and T_2), and (T_0) is time period of zero vector. Switching modes of SVPWM in first sector (I) are sketched in Fig. 3.c, where time period (T_1 and T_2) of active vector(V_1 and V_2)is symmetrically split into two portions and time period (T_0) for both zero vectors (V_0 and V_7) is equally divided. Therefore, the sequence (V_0-V_1-V_2-V_7-V_7-V_2-V_1-V_0) is corresponding to the switching in the time period of space vector pulse width modulation. Consequently, the switching losses and current harmonics are minimized as a result of applied switching sequence which presents one switches during of switching mode switches. The switching time of SVPWM depends on the time period (T_1, T_2, and T_0) as given in equations (9, 10, and 11) for each sector [18].

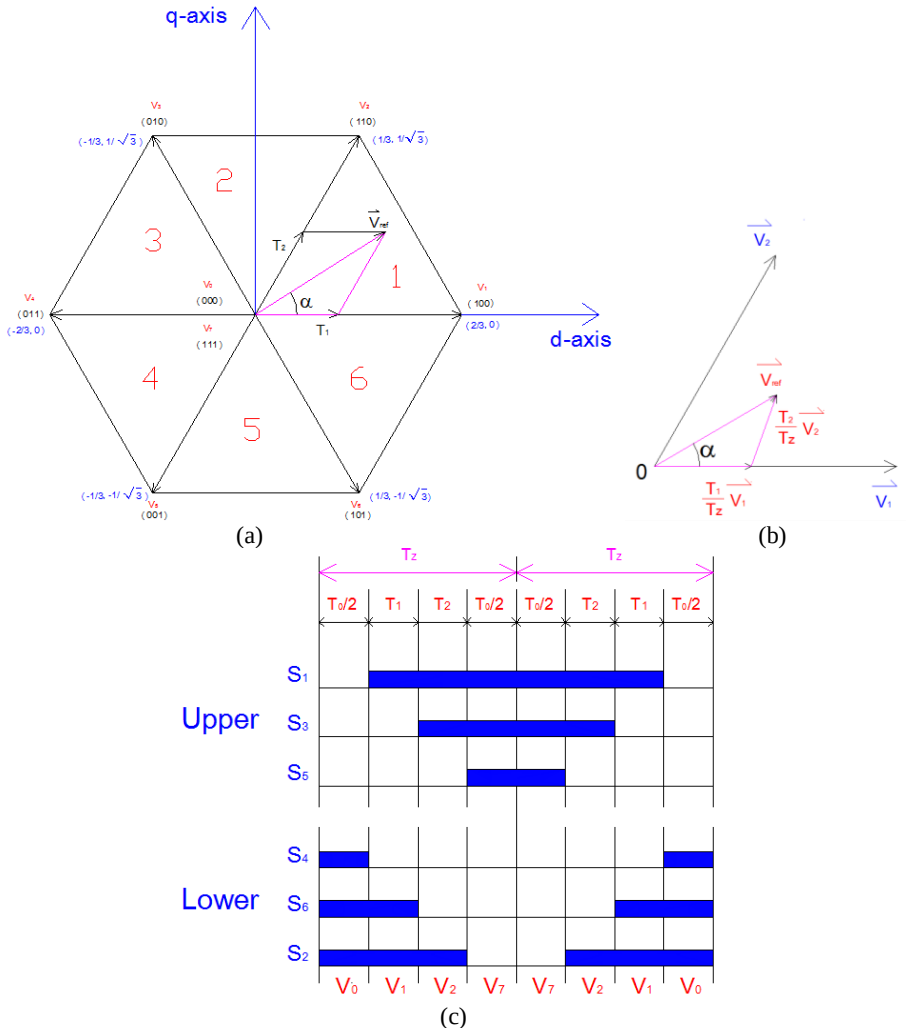


Figure 3: Two-level SVPWM. (a) Sectors and voltage vectors. (b) Created of reference voltage. (c) Switching modes in sector-I

$$T_1 = \frac{\sqrt{3}T_z|\overrightarrow{V_{ref}}|}{V_{dc}}\left(\sin\frac{n}{3}\pi\cos\alpha - \cos\frac{n}{3}\pi\sin\alpha\right) \quad (9)$$

$$T_2 = \frac{\sqrt{3}T_z|\overrightarrow{V_{ref}}|}{V_{dc}}\left(-\cos\alpha\sin\frac{n-1}{3}\pi + \cos\frac{n-1}{3}\pi\sin\alpha\right) \quad (10)$$

$$T_0 = T_z - T_1 - T_2 \quad (11)$$

2.3.2 A Three-Level SVPWM For SAPF

Reference voltage(V_{ref}) in a space reference frame can be provided from three phase supply voltage($V_{abc}\ stationary\ reference\ frame$)at fundamental frequency (f_1) by employed Clarke transformation($V_{\alpha\beta}\ stationary\ reference\ frame$). Phase leg of three phase three

level neutral point clamped converter operation comprised of three switching status (Positive, Negative, and Zero), thereby this inverter is called three level NPC inverter. Accordingly, overall of switching statuses of three phase three level diode clamped inverter are twenty-seven statuses. In this way, by utilize of three zero vectors, twelve small vectors, six middle vectors, and six large vectors, it can appreciate twenty-seven space voltage vectors. As shown in Fig. 4.a, for the operation of the space voltage vectors, this spatial split into six large portion (I-VI) all of them are sectioned into four small sectors (A, B, C, and D) as clarified in Fig. 4.b.

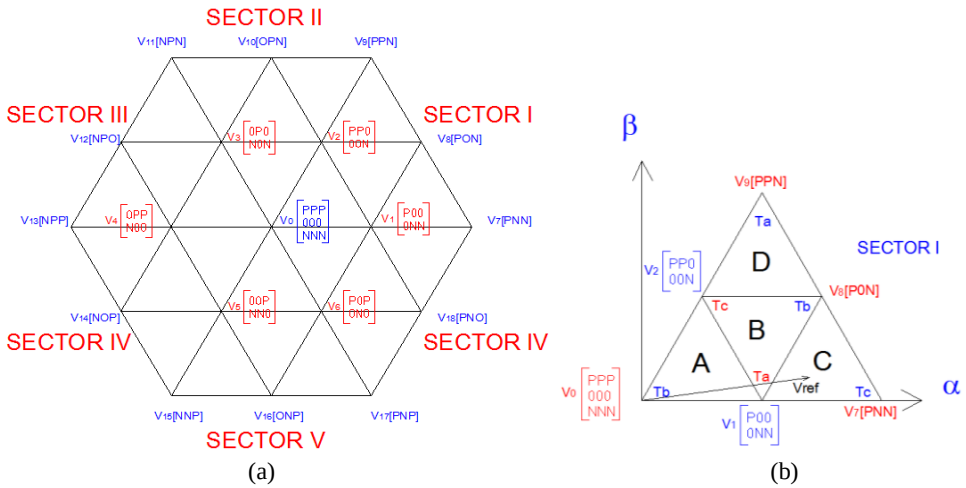


Figure 4: (a) Switching statuses for diode clamped inverter. (b) Division of first sector (I)

From Fig. 4.a, the first big sector (I) angle is$(0^{\circ}-60^{\circ})$, the second big sector (II) angle is $(60^{\circ}-120^{\circ})$, the third big sector (III) angle is $(120^{\circ}-180^{\circ})$, the fourth big sector (IV) angle is $(180^{\circ}-240^{\circ})$, the fifth big sector (V) angle is $(240^{\circ}-300^{\circ})$, and the last sector is sixth big sector (VI) with angle $(300^{\circ}-360^{\circ})$. As clarified in Fig. 4.b, by employed different vectors, the four small sectors (A, B, C, and D) can be achievement. In this case, when reference voltage (V_{ref}) is lying in triangle (C), then the reference voltage $(V_{ref})$is made-up of vectors $(V_1, V_7, and\ V_8)$, according to the rule of adjacent triangle vectors. To calculate the time duration of three closest voltage vectors, it can be utilize the equations (12-15) when reference voltage is placed in sector-I as demonstrated in Fig. 4.b.

Zone A: $V_{ref}T_s = T_aV_1 + T_bV_0 + T_cV_2$ (12)
Zone B: $V_{ref}T_s = T_aV_1 + T_bV_8 + T_cV_2$ (13)
Zone C: $V_{ref}T_s = T_aV_1 + T_bV_8 + T_cV_7$ (14)
Zone D: $V_{ref}T_s = T_aV_9 + T_bV_8 + T_cV_2$ (15)

Switching time duration of each voltage vector is lists in Table 2 when reference voltage is placed in the first sector (I).

Table 2: Time duration of voltage vectors in first sector (I)

Zone	T_a	T_b	T_c
A	$T_s\left[2K\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$T_s\left[1-2K\,sin\left(\frac{\pi}{3}+\theta\right)\right]$	$T_s[2K\sin(\theta)]$
B	$T_s[1-2K\sin(\theta)]$	$T_s\left[2K\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	$T_s\left[1-2K\sin\left(\frac{\pi}{3}-\theta\right)\right]$
C	$T_s\left[2-2K\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$T_s[2K\sin(\theta)]$	$T_s\left[2K\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$
D	$T_s[2K\sin(\theta)-1]$	$T_s\left[2K\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$T_s\left[2-2K\sin\left(\frac{\pi}{3}+\theta\right)\right]$

Where (T_s) is sampling time of switching time, $(T_a, T_b \text{and } T_c)$ are time duration of voltage vectors $(V_a, V_b \text{and } V_c)$, (K) is $(\frac{2|V_{ref}|}{\sqrt{3}V_{dc}})$, (θ) is angle from(α) axis to reference voltage, $|V_{ref}|$ is absolute value of reference vector, and (V_{dc}) is dc-reference voltage. Likewise, for various big sectors (I-VI), the time period of three adjacent voltage vectors can be calculated [19].

3. STRATEGY OF THE PROPOSED DC-UNBALANCE CONTROL

The scheme of the proposed control algorithm is demonstrated as seen in Fig. 5. Park's transformation is dedicated to convert load currents and inverter currents into the d-q rotating reference frame by exploited phase locked loop, thereby the load and inverter currents orientation will be aligned with the three phase voltage supply.

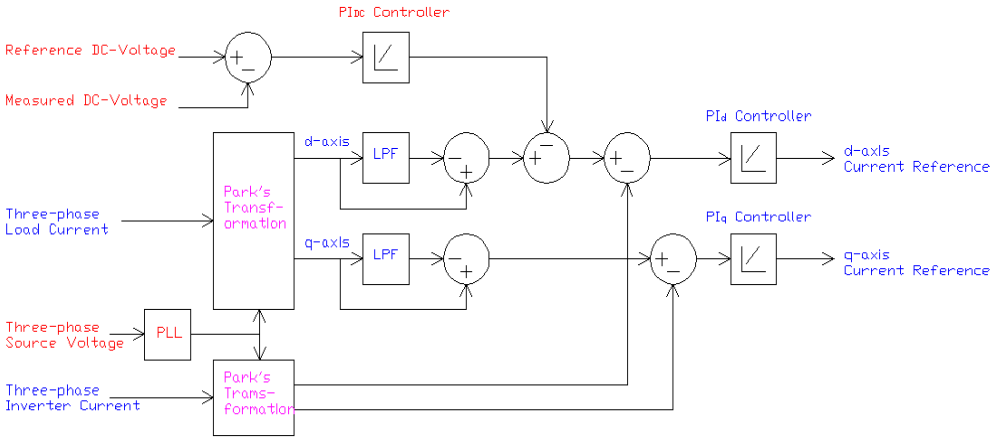


Figure 5: DC-unbalance control strategy

The direct-axis and quadrature axis represented the real and reactive components of three phase load currents with the fundamental frequency [20]. To keep-up the voltage of DC-bus capacitors invariable, the PI_{DC} controller is employed. Consequently, the active power passing through the shunt active harmonic filter and the currents of d-axis and q-axis are regulated by devoted PI_d and PI_q current controller. This achieved by comparing the actual voltage of the DC-bus capacitors with the desired voltage of DC-bus capacitors. The PI_{DC} controller receive the difference voltage which is the active current necessitated to keep the voltage of DC-bus capacitors [21]. The output of PI_{DC} controller is a part of current harmonic components of d-axis reference to produce the entire current with d-axis for the

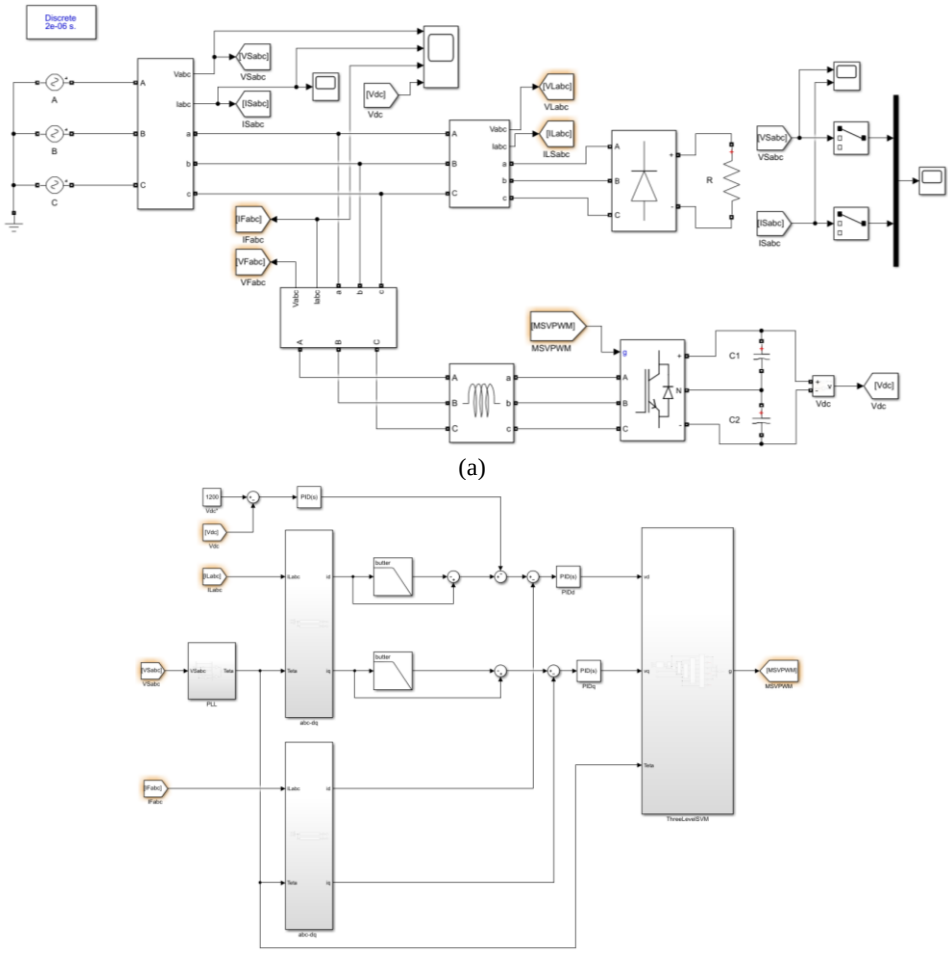
reference current controller. The DC-link capacitor acts as storage of energy to provide the active power during the transient time and to keep the DC-link voltage in steady state period with a little ripple [22].

4. SIMULATION RESULTS AND DISCUSSION

The presented work of MSVPWM technique based- SAPF for three-phase three-level diode clamped inverter fed compensation currents at nearest point from the load renowned as point of common coupling for source currents THD percent mitigation is simulated via MATLAB/SIMULINK power system as illustrated by Fig. 6. To evidence the efficiency of the presented control technique, a simulation work has been carried out on non-linear loads were operated at balanced and unbalanced power system voltage condition dedicated the parameters as tabulated in Table 3.

Table 3: Parameters of Simulation for Proposed Model

Parameter	**Value**
Source Voltage/Phase(rms)	220 V
Supply frequency	50 Hz
Non-linear Loads	Diode Rectifier (Three-phase) and Resistance Load(30 Ω)
DC-reference Voltage	1200 V
DC-Link Capacitor Voltage/Capacitor	500 V
DC-Link Capacitance/Capacitor	1500μF
Filter Inductance	2mH



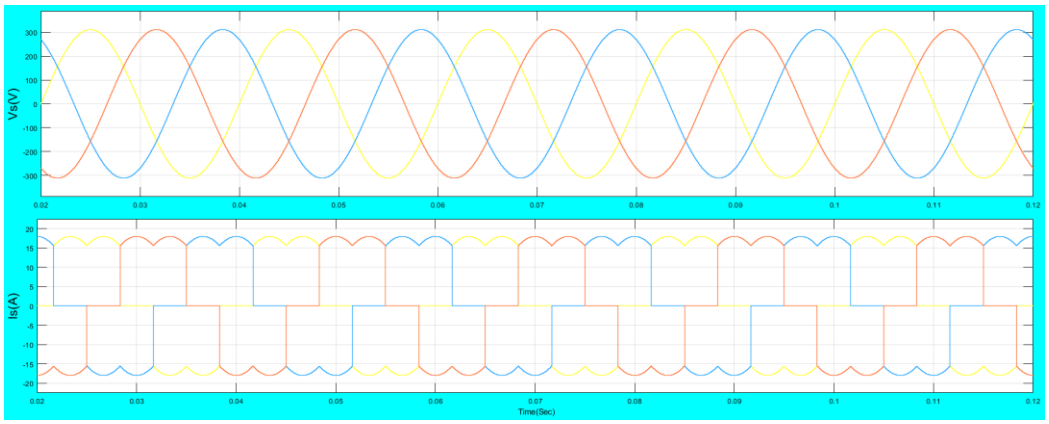
(a)

(b)

Figure 6: Simulation of Proposed Model Using MATLAB/SIMULINK. (a) SAPF. (b) MSVPWM

4.1 Simulation Results With and Without MSVPWM Based-SAPF Under Balanced Source Voltage

Fig.7.ashows the supply voltages and source currents without SAHF and Fig.7.c show the waveforms of supply voltages, source currents, compensating currents, and DC-bus capacitor voltages with MSVPWM based-SAPF. Supply currents (I_S)with MSVPWM based-SAPF are ideal sinusoidal and have same phase angle with source voltage (V_S)when compared with the input waveforms of source voltages and currents as demonstrated in Fig. 7.a. The DC-bus capacitor voltage with MSVPWM based-SAPF contained little ripple compared to CSVPWM based-SAPF as seen in Fig. 7.c and Fig. 7.b respectively in steady-state time.



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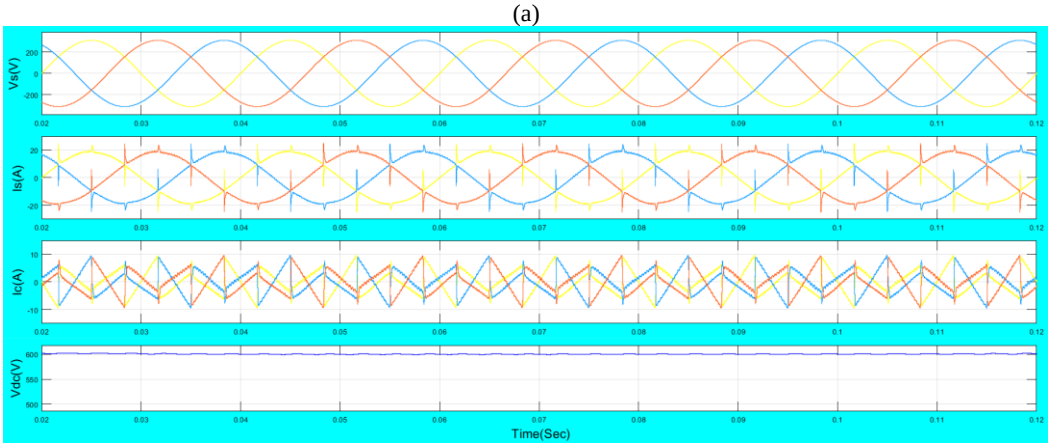

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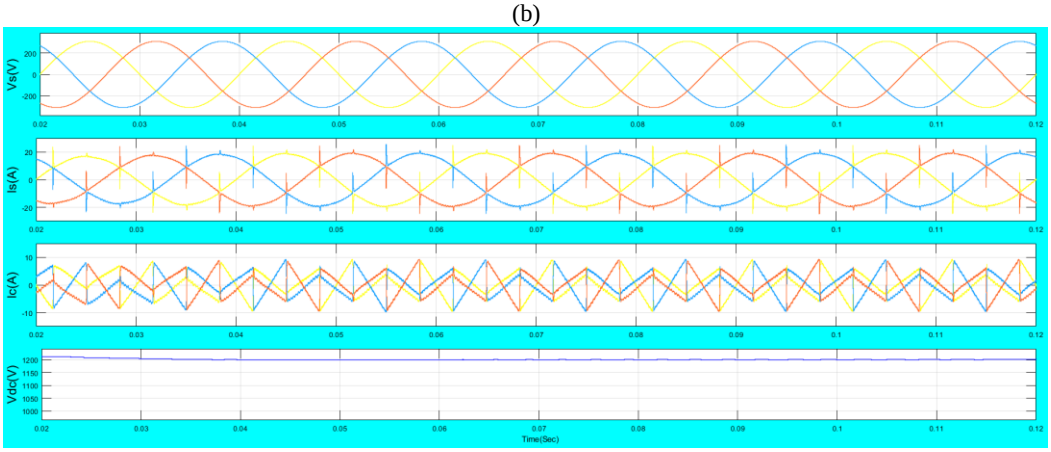
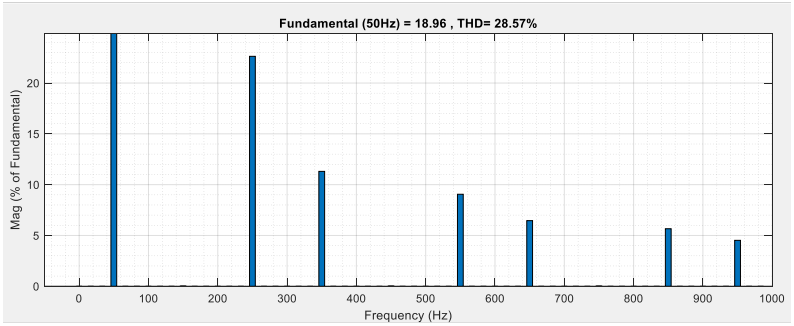


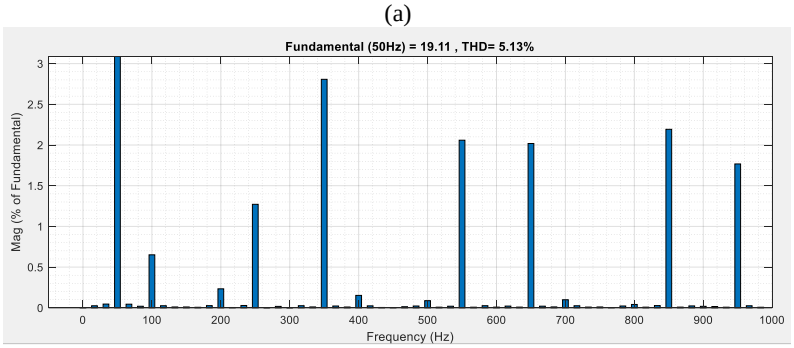
(C)

Figure 7: Simulation Results of Waveforms under Balanced Condition. (a) Without Compensation. (b) With CSVPWM. (c)With MSVPWM

Fig.8.a,exhibit the analysis of Fast Fourier Transform (FFT) for supply currents without compensation currents(I_C) by SAPF and Fig. 8.cshows the Fast Fourier transform of source current (I_S)with compensation current by MSVPWM based-SAPF. The source current with applied MSVPWM based-SAPF achieved a significant mitigation in 3.58% THD compared to 28.57% THD without to current compensation by SAPF and better performance than 5.13% THD when employed conventional SVPWM as in Fig.8.b.



(a)



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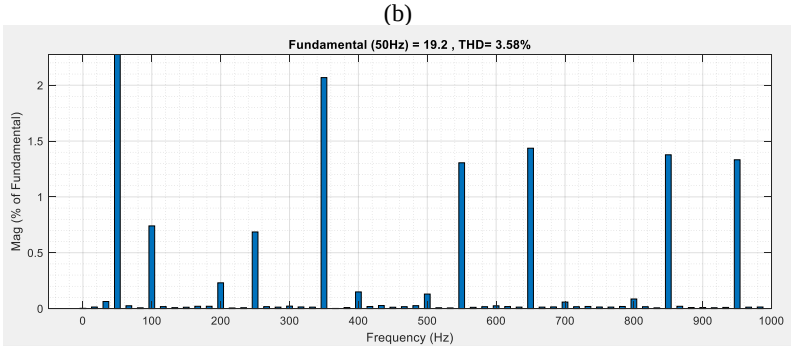
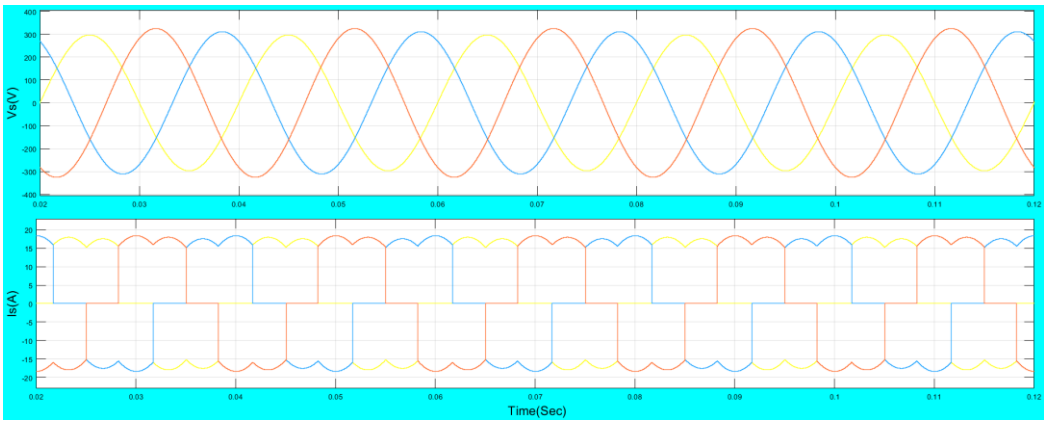


(c)

Figure 8: FFT Analysis of Source Current under Balanced Condition. (a) Without Compensation. (b) With CSVPWM. (c) With MSVPWM.

4.2 Simulation Results With and Without MSVPWM Based-SAPF Under Unbalanced Source Voltage

MSVPWM technique based-SAPF was tested under unbalanced power system distributed phase voltages as($V_a = 210\ V, V_b = 220\ V, and\ V_C = 230\ V$). Fig. 9.a shows the supply voltages and source currents without MSVPWM based-SAHF and Fig. 9.c display the waveforms of supply voltages, source currents, compensating currents, and DC-bus capacitor voltages with MSVPWM based-SAPF. Supply currents with MSVPWM based-SAPF are ideal sinusoidal and has same phase angle with supply voltage when compared with the input waveforms of voltages and currents respectively shown by Fig. 9.a.The voltage of DC-bus capacitor with MSVPWM based-SAPF comprise very small ripple compared to CSVPWM based-SAPF as evident in Fig. 9.c and Fig. 9.b respectively in steady-state period.



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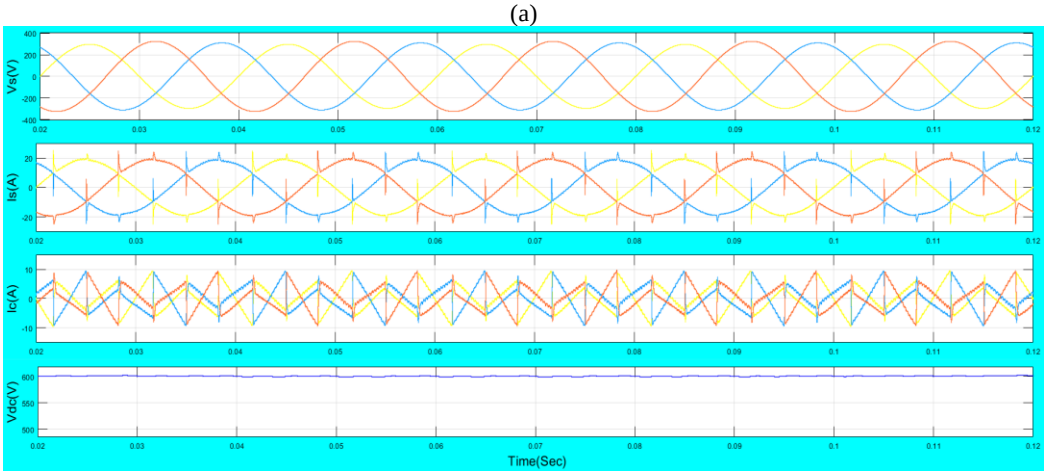
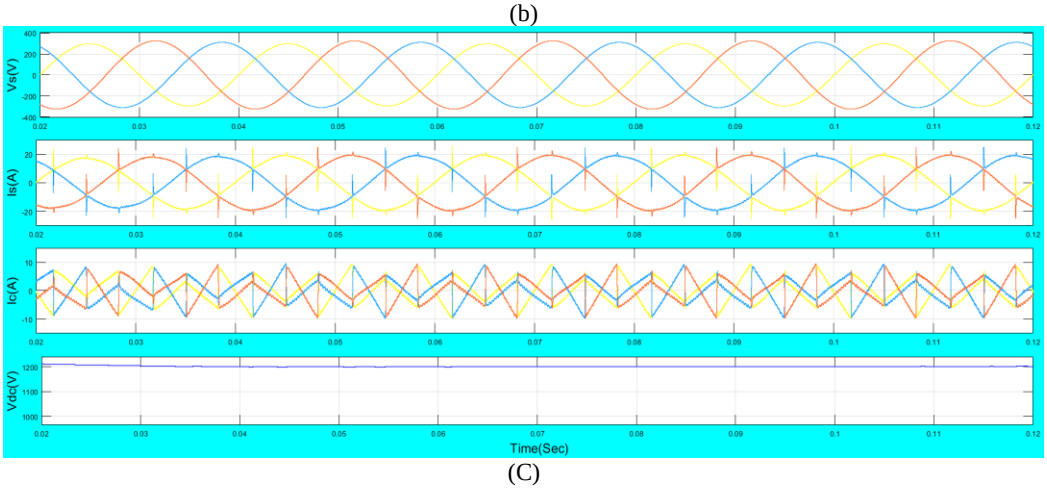


(b)



(C)

Figure 9: Simulation Results of Waveforms under Balanced Condition. (a) Without Compensation. (b) With CSVPWM. (c) With MSVPWM

Fig. 10.a.viewsthe analysis of Fast Fourier Transform (FFT)for supply current under unbalanced source voltages without compensation currents by SAPF and Fig. 10.c. shows the fast Fourier transform of source current under unbalanced source voltages with compensation current by SAPF. The source current with applied MSVPWM based-SAPF achieved a significant mitigation in 3.96% THD compared to 29.76%

THD without to current compensation by SAPF and better performance than 5.45% THD when employed conventional SVPWM as in Fig.10.b.

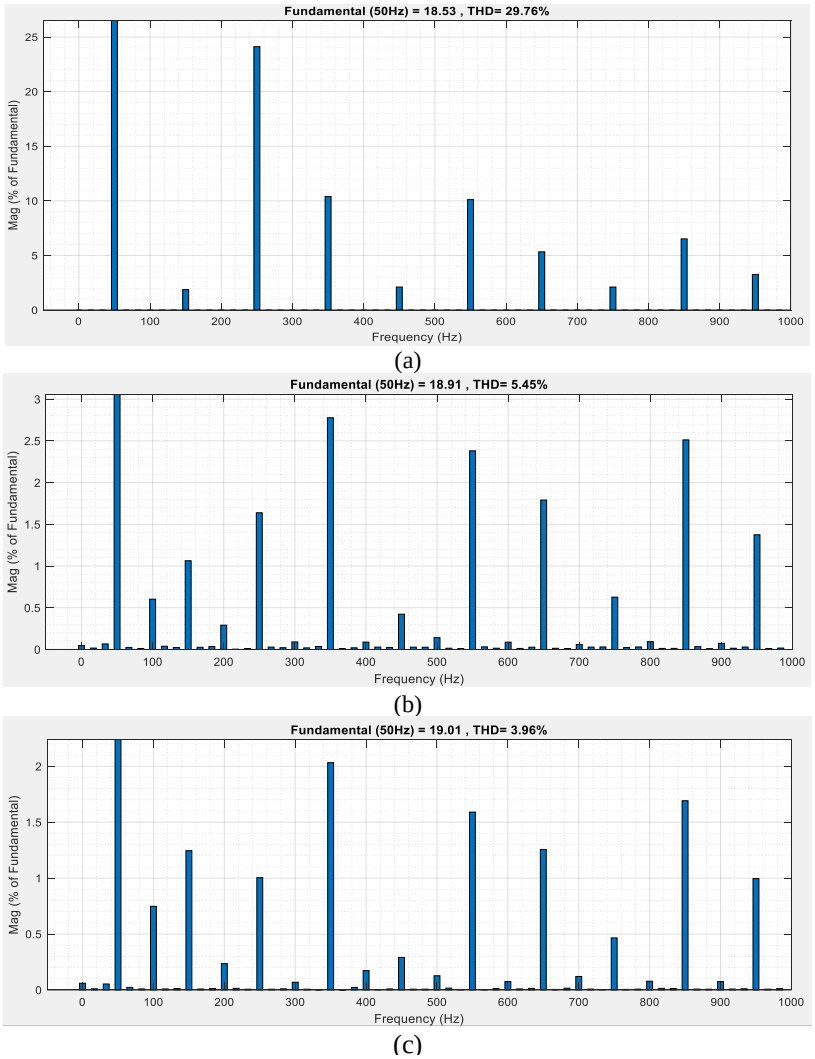


Figure 10: FFT analysis of Source Current under Unbalanced Condition. (a) Without Compensation. (b) With CSVPWM. (c) With MSVPWM.

Table 4: Comparative analysis of supply current THD%

Supply Voltages	Without SAPF	With CSVPWM-SAPF	With MSVPWM-SAPF
Balanced	28.57%	5.13%	3.58%
Unbalanced	29.76%	5.45%	3.96%

5. CONCLUSION

To mitigation of source currents THD% in power system distribution network, a MATLAB/Simulink model of three-level SVPWM technique has been proposed with three-phase multi-level diode clamped (DC) inverter based-shunt active harmonic filter (SAHF). The supply currents THD %in consequence of various pulse width modulation (PWM) control techniques are estimated and compared under balanced and unbalanced source voltages by

FFT analysis. The simulation results indicated that the reduction of THD% from 28.57% to 5.13% for balanced supply voltage and from 29.76% to 5.45% for unbalanced source voltage by using conventional SVPWM technique based-SAPF. The proposed three-level SVPWM based-SAPF leads to further reduction in supply current THD% from 28.57% to 3.58% for balanced supply voltage and 29.76% to 3.96% for unbalanced source voltage. The simulation results under different cases as evident in table 4 illustrated that the proposed work employed MSVPWM based SAPF is better than CSVPWM method and achievement performance accepted by harmonics standard IEEE 519 (THD % less than 5%)[23]. The DC voltage of link capacitors with MSVPWM based-SAPF maintained at desired voltage with tiny ripple during the steady-state.

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