The Journal of Engineering Research (TJER) Vol. 14, No. 1 (2017) 74-84

Performance Comparison of Digital Circuits Using Subthreshold Leakage Power Reduction Techniques

B. Kalagadda[*, a], N. Muthyala[b] and K.K. Korlapati[c]

[*a, b] *Department of Electronics and Communication Engineering, Kakatiya University College of Engineering and Technology, Kakatiya University, Warangal-506001, Telangana, India.*
[c] *Department of Electronics and Communication Engineering, National Institute of Technology, Warangal-506004, Telangana, India.*

Received 8 June 2015; Accepted 2 October 2016

Abstract: Complementary metal-oxide semiconductors (CMOS), stack, sleep and sleepy keeper techniques are used to control sub-threshold leakage. These effective low-power digital circuit design approaches reduce the overall power dissipation. In this paper, the characteristics of inverter, two-input negative-AND (NAND) gate, and half adder digital circuits were analyzed and compared in 45nm, 120nm, 180nm technology nodes by applying several leakage power reduction methodologies to conventional CMOS designs. The sleepy keeper technique when compared to other techniques dissipates less static power. The advantage of the sleepy keeper technique is mainly its ability to preserve the logic state of a digital circuit while reducing subthreshold leakage power dissipation.

Keywords: Sub-threshold leakage, Stack, Sleep, Sleepy keeper, Static power.

مقارنة أداء الدوائر الرقمية باستخدام تقنيات الحد الأدنى لتقليل تسريب القدرة

ب. كلاجادا[*،a]، ن. موثيالا[b]، ك. كورلاباتي[c]

الملخص: الحد الأدنى للتسريب هو مكون أساسي للتسريب في دوائر VLSI. التقنيات مثل CMOS، التكوم ، النعاس وحارس النعاس يمكن استخدامها للتحكم في الحد الأدنى للتسريب. هذه التقنيات الفعالة تقلل القدرة الكلية المهدرة عند تصميم دوائر رقمية بقدرة منخفضة. في هذه المقالة؛ الخصائص للدوائر الرقمية مثل المعاكس و بوابة NAND بمدخلين والجامع النصفي يتم تحليلها ومقارنتها بتكنولوجيات مختلفة مثل ٤٥ نانو متر، ١٢٠ نانو متر، ١٨٠ نانو متر وذلك بتطبيق منهجيات تقليل تسريب القدرة لتصميمات CMOS التقليدية. عند مقارنة تقنية حارس النعاس بالتقنيات الأخرى وجد أنها فقدت قدرة ساكنة أقل. الميزة لتقنية حارس النعاس هو الحفاظ على الحالة المنطقية للدائرة الرقمية أثناء تقليل الحد الأدنى للقدرة المهدرة.

الكلمات المفتاحية: الحد الأدنى للتسريب، التكوم، النعاس، حارس النعاس، القدرة الساكنة.

* Corresponding author's email: kalagaddaashu@kakatiya.ac.in

1. Introduction

Integrated circuit technology enables the innovative devices and systems that change the essence of life. The continuous development of high performance integrated circuits has led to an explosion in communication and computation systems. Major concerns with very-large-scale integration (VLSI) designs recently have shifted to power considerations along with area and speed. Power management for VLSI design has become vital due to a reduction in the geometry of transistors and also exponential growth in the number of transistors on a single chip. This trend developed because of special portable devices and applications. The change in technology has been the result of development in VLSI techniques, which has emerged as a rapidly growing technology influencing the world in encouraging innovation. Improvements in manufacturing have led to ever-smaller transistors which can accommodate a greater number of transistors on a chip. The integrated circuits industry has increased the functionality of larger chips by allowing a steady path for constantly shrinking device geometries. Each new generation has approximately doubled logic circuit density and increased performance by about 40%.

Due to advanced IC technology, the minimum feature size of VLSI circuitry continues to decrease. The feature size of transistors has entered the nano-scale region due to its shrinking capacity. The transistors with smaller feature sizes have the capability of increasing the speed of the circuit and yield of manufactured chips. The latter is due to the smaller silicon area of the chip, which lowers the average number of defects per chip. VLSI chip manufacturers effectively utilize the advantages of possible reductions in feature size by scaling (shrinking) the existing designs of integrated circuits (ICs) (Borkar 1999). The better performance and rich feature sets on a single chip have evolved with an increase in integration level. As the technology scaling has continued, many design techniques mainly from the field of power management must be employed in order to attain a balanced design to meet end user needs while maintaining the performance trend of a VLSI system. The need to dissipate low power for electronic devices in Order to conserve battery life and meet packaging reliability constraints has recently arisen. In portable devices, the reduction in power consumption is essential for improving battery life and reliability and reducing heat removal costs mainly in high performance systems.

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS devices possess important characteristics like high noise immunity and low static power consumption. In VLSI circuits, CMOS technology has become the most frequently used technology for implementation purposes because CMOS allows for a high density of logic functions on a chip. Recently much progress has been made in estimating power dissipation; power dissipation has thereby driven the design of new low power systems, and accurate and efficient power estimation techniques have been used (Bursky 1995). CMOS transistors, as they constantly switch, dissipate power. Due to this feature, dynamic power consumption is related to the number and size of transistors and also to the rate at which they switch. When the feature size shrinks below 180nm, the transistors leak a significant amount of current even in the off state. The chips, therefore, draw static power even when they are idle.

The main challenge of VLSI design is to make a good tradeoff between performance and power for a particular application. To achieve this, the methods, which reduce power leakage, have to be adopted with conventional CMOS circuits. This paper aims to detail a method to reduce sub-threshold leakage power since it is the most dominant among all the leakages in the deep sub-micron technologies (Saini and Mishra 2012). In this paper, several leakage reduction methodologies like stack, sleep, and sleepy keeper techniques were applied with the conventional digital CMOS circuits like an inverter, a two-input NAND gate, and a half adder in 180nm, 120nm, and 45nm technologies. The performance of these circuits was evaluated among those leakage reduction techniques.

The current paper is organized as follows: Section 2 describes the kinds of power dissipation, section 3 discusses several leakage power reduction mechanisms, section 4 presents the results, and section 5 concludes the paper.

2. Power Dissipation

Power dissipation in CMOS circuits is generally due to dynamic dissipation and static dissipation. The total power in a circuit is given by

$$P_{total} = P_{dynamic} + P_{static} \quad (1)$$

where P_{total} is the total power dissipation of the circuit, $P_{dynamic}$ is the dynamic power consumption and P_{static} is the static power consumption.

2.1 Dynamic Power Dissipation

The dynamic power dissipation mainly occurs due to the switching activity of the transistors and the continuous charging and discharging of the MOS capacitors. This also occurs due to short-circuit current when both pMOS and nMOS stacks are partially ON.

2.2 Static Power Dissipation

The static power dissipation is mainly due to the sub-threshold leakage current through OFF transistors, gate leakage through gate dielectric material, junction leakage from source or drain diffusions, and contention current in ratioed logic circuits. The static power exists even when the chip is not in active mode. The power is also described in terms of active, standby, and sleep modes. The power that is utilized when the chip is ON is the active power, which is dominated by switching activity. When the chip is in a non-active state, standby power exists. The standby power is set by leakage in case of halted clocks and disabled ratioed logic circuits. The sleep mode intends to avoid leakage by disconnecting the power supply to unwanted circuits on a chip. In nanometer technologies, nearly one-third of the total power is considered leakage power.

Since sub-threshold leakage is considered the most dominant of all leakages, a detailed explanation of it is given in the next section.

2.3 Subthreshold Leakage Power

Subthreshold leakage is the dominant source of static power. Subthreshold leakage or conduction occurs due to thermal emission of carriers over the potential barrier, which is set by the threshold (Boray *et al*. 2007). Sub-threshold leakage current flows even when a transistor is nominally OFF. Sub-threshold leakage increases due to the downscaling of threshold voltages. In weak inversion, below threshold voltage the transistors are not completely OFF and the sub-threshold current relies on threshold voltage. The sub-threshold leakage increases exponentially with a decrease in threshold voltage or rises with temperature, which is a major problem for chips using low supply and threshold voltages and operating at high temperatures. The sub-threshold leakage current is given as:

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{to} + \eta V_{ds} - k_\gamma V_{sb}}{nV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \quad (2)$$

where I_{ds0} is the current at threshold and is dependent on process and device geometry.

$$I_{ds0} = \beta V_T^2 e^{1.8} \quad (3)$$

The process-dependent term n is affected by depletion region characteristics; the term ηV_{ds} indicates a reduction of threshold voltage by drain-induced barrier lowering; V_{gs}, V_{ds}, and V_{sb} indicate gate-to-source, drain-to-source, and source-to-bulk voltages of a metal-oxide-semiconductor (MOS) transistor, respectively; V_T is the thermal voltage; V_{to} indicates a zero-based threshold; k_γ is the body effect coefficient, and the $e^{1.8}$ term is found empirically. The sub-threshold current path is shown in Fig. 1. Leakage generally accounts for a third of the total active power when low

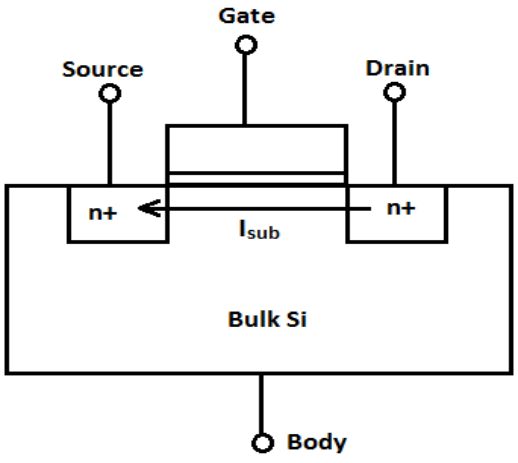

Figure 1. Subthreshold leakage current path.

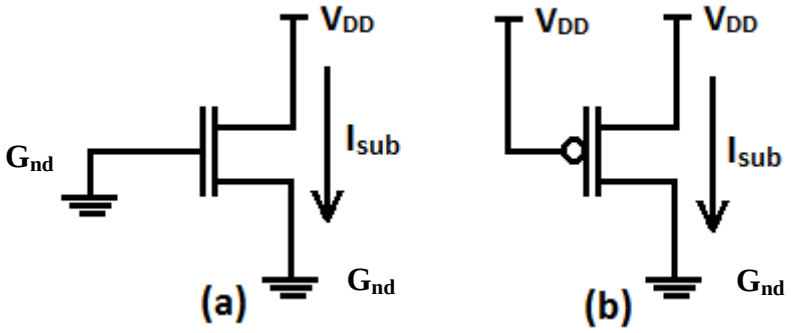

Figure 2. Method to measure subthreshold leakage current through (a) NMOS transistor, and (b) PMOS transistor.

threshold voltages and thin gate oxides are applied in nanometer processes. Except in very low power applications, leakage is insignificant at above 180 nm. In 45 nm, high–K gate dielectrics is used so that sub-threshold leakage is not dominated by gate leakage. Necessary reduction techniques are then employed to reduce sub-threshold leakage.

Static power comes from the leakage and circuits with a path from the VDD (voltage drain) to the GND (ground drain). When operated at high threshold voltages, the complementary CMOS gates dissipate almost zero static power, so the circuits consume low power. The leakage increases as feature size decreases making static power consumption dominant along with dynamic power.

2.4 Method to Measure Subthreshold Leakage Current

In a general metal–oxide–semiconductor field-effect transistor (MOSFET) sub-threshold current is found by switching off the gate terminal. The current from VDD to GND in this case is the subthreshold leakage current. The scenario is shown in Fig. 2.

3. Reduction Techniques of Subthreshold Leakage

The low power design is mainly to reduce the predominant factor of power dissipation. So in nanometer processes, overall leakage becomes an important design constraint (Roy *et al*. 2003). The sub-threshold leakage which is dominant in leakage or static power dissipation is to be reduced. The following are techniques to reduce sub-threshold leakage so that power dissipation can be decreased, which is a VLSI design constraint.

3.1 Stack Technique

The leakage trough of two or more transistors is reduced on account of the stack effect. Stacks with three or more OFF transistors have even lower leakage levels. A circuit can be stacked into two half-width size transistors but propagation delay rises with number of transistors (Johnson *et al*. 2002). Figure 3 shows the stack technique. In this technique, the pMOS transistors' width in the pull-up network is divided and stacked into two half-width size transistors. Similarly, the width of the nMOS transistors in the pull-down network is also divided and stacked into two half-width size transistors. The major disadvantage with this technique is that it increases the overall propagation delay.

3.2 Sleep Technique

The sleep technique uses sleep transistors with high threshold voltages. Figure 4 depicts the sleep technique. The sleep signal is used to

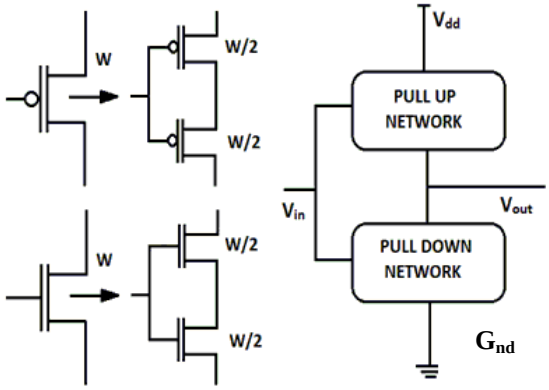

Figure 3. Stack technique.

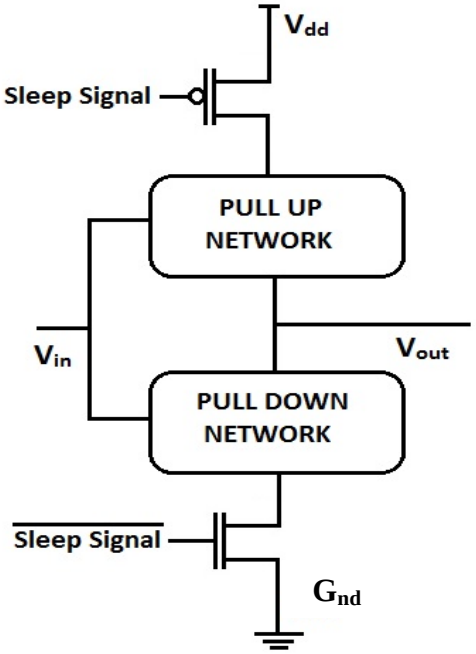

Figure 4. Sleep technique.

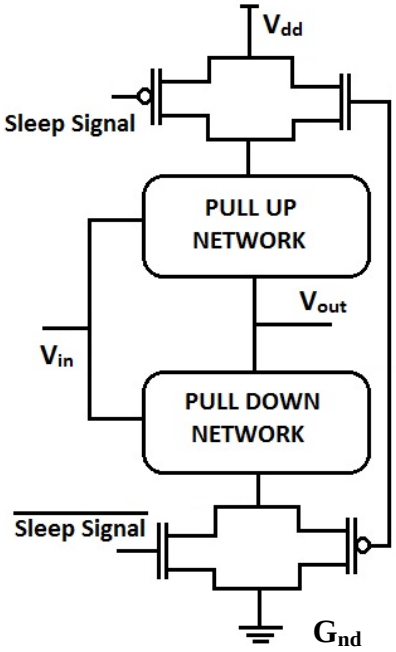

Figure 5. Sleep keeper technique.

drive the sleep transistors. In this technique, the pull-up and pull-down networks are separated from supply and ground respectively by sleep pMOS and nMOS transistors (Kumar et al., 2012). In sleep state, the transistors are OFF which reduces the sub-threshold leakage current. This technique comes under the state destructive technique. This implies that the circuit state is lost but the leakage is reduced. The disadvantages of this technique are the destruction of the state of the circuit and the fabrication of high threshold voltage sleep transistors with conventional MOS transistors on a single-die required triple well process.

3.3 Sleepy Keeper Technique

The sleepy keeper technique is a state-preserving technique. It has advantageous characteristics over the sleep technique. Figure 5 describes the sleepy keeper technique. In this technique, high threshold voltage pMOS and nMOS transistors are additionally used. This is the same as the sleep technique, but the additional high threshold voltage nMOS transistor is placed parallel to the sleep transistor. Similarly, the additional high threshold voltage pMOS transistor is placed parallel to the sleep nMOS transistor. When the circuit is in sleep mode, the high threshold voltage nMOS transistor is connected to the supply and the high threshold voltage pMOS transistor is connected to ground. The sleepy keeper technique is advantageous when compared to all other techniques. It reduces the sub-threshold leakage current along with maintaining its state.

4. Results and Discussion

The performance of digital circuits like inverters, two-input NAND gates, and a half adder have been studied in the current article. MICROWIND (MICROWIND, Toulouse, France) was used for layout and simulation purposes using a BSIM4 model in 45nm, 120nm, and 180nm technologies. Stack, sleep and sleepy keeper sub-threshold reduction techniques were used to calculate dynamic power dissipation, static power dissipation, and propagation delay at 27°C. The channel widths and lengths were maintained according to the technology node. The results were compared against the parameters obtained with conventional CMOS designs.

Figure 6 shows the layout of a conventional CMOS inverter. Figures 7–9 correspond to the layouts of the inverter with stack, sleep, and sleepy keeper techniques, respectively, which were simulated in 45nm technology.

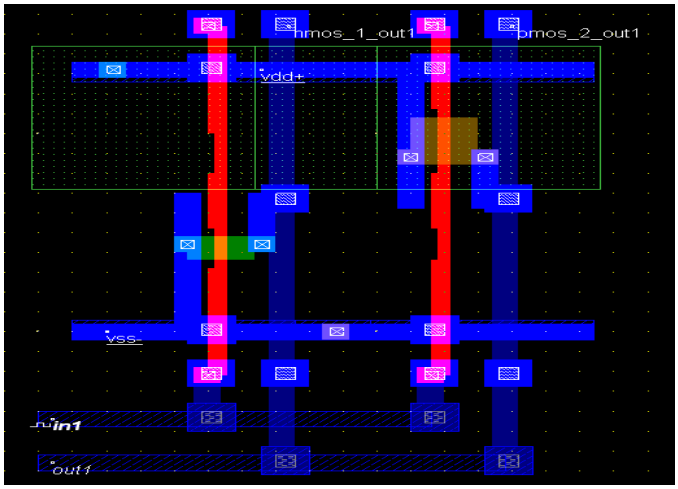

Figure 6. Layout of conventional CMOS Inverter 45nm technology.

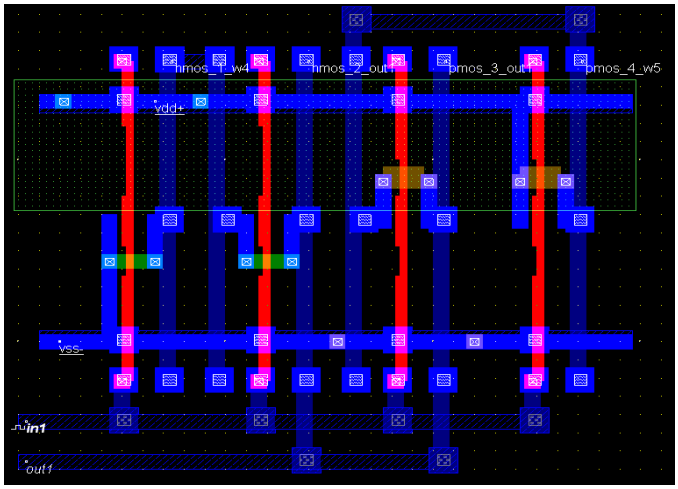

Figure 7. Inverter layout with stack technique in 45nm technology.

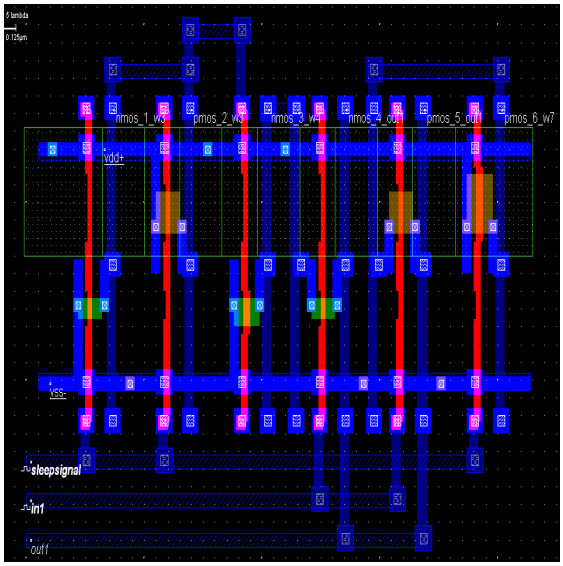

Figure 8. Inverter layout with sleep technique in 45nm technology.

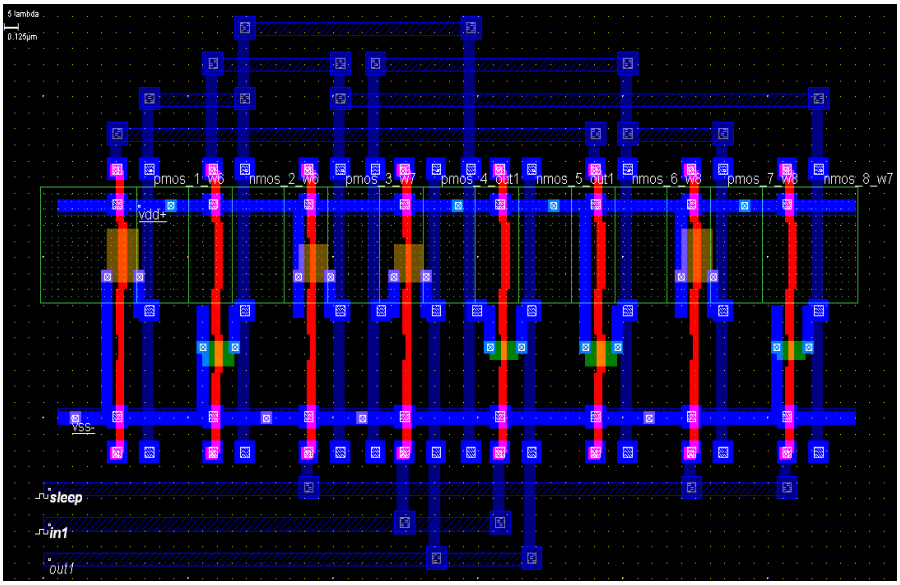

Figure 9. Inverter layout with Sleepy keeper technique in 45nm technology.

Table 1 compares the performance of inverter using 180, 120 and 45 nm technologies with different leakage reduction mechanisms applied on a conventional CMOS inverter (Fig. 10).

Table 1. Inverter performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

Technology	180nm		120nm		45nm	
Technique	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Sub-threshold Leakage Power (µW)
Conventional CMOS	9.917	2.12	2.473	0.469	0.078	0.021
Stack	9.672	1.919	2.425	0.426	0.073	0.018
Sleep	7.78	1.723	1.072	0.329	0.086	0.015
Sleepy Keeper	9.123	1.694	2.364	0.271	0.094	0.013

Table 2 compares the performance of a two input NAND gate in 180, 120 and 45 nm technologies with different leakage reduction mechanisms applied on a conventional CMOS two input NAND gate and is depicted in Fig. 11.

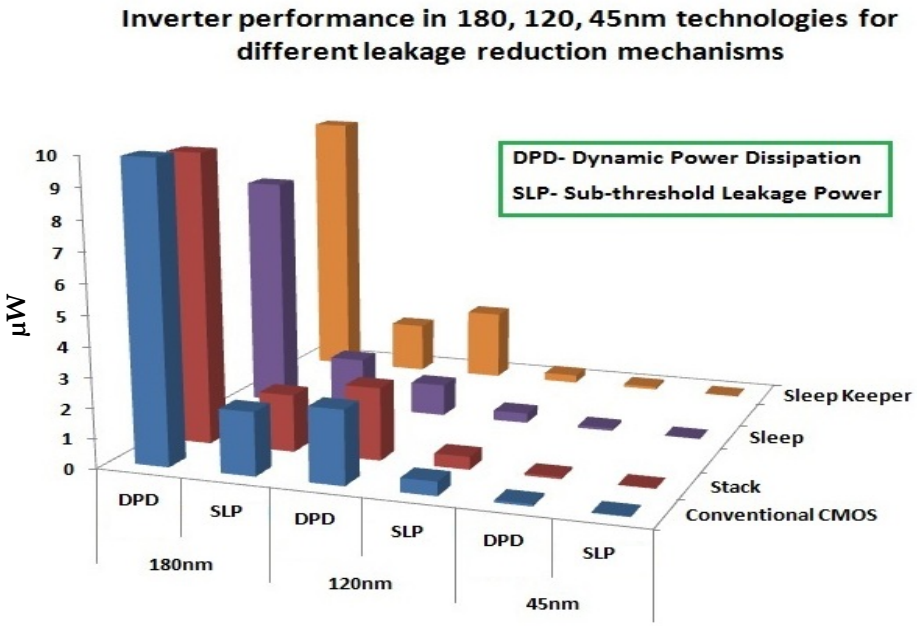

Figure 10. Inverter performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

Table 2. Two input NAND gate performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

Technology	180nm		120nm		45nm	
Technique	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)
Conventional CMOS	12.01	2.921	3.661	0.737	0.121	0.030
Stack	11.693	2.465	2.978	0.621	0.119	0.026
Sleep	9.875	1.992	1.708	0.507	0.131	0.023
Sleepy Keeper	11.01	1.802	2.905	0.391	0.134	0.019

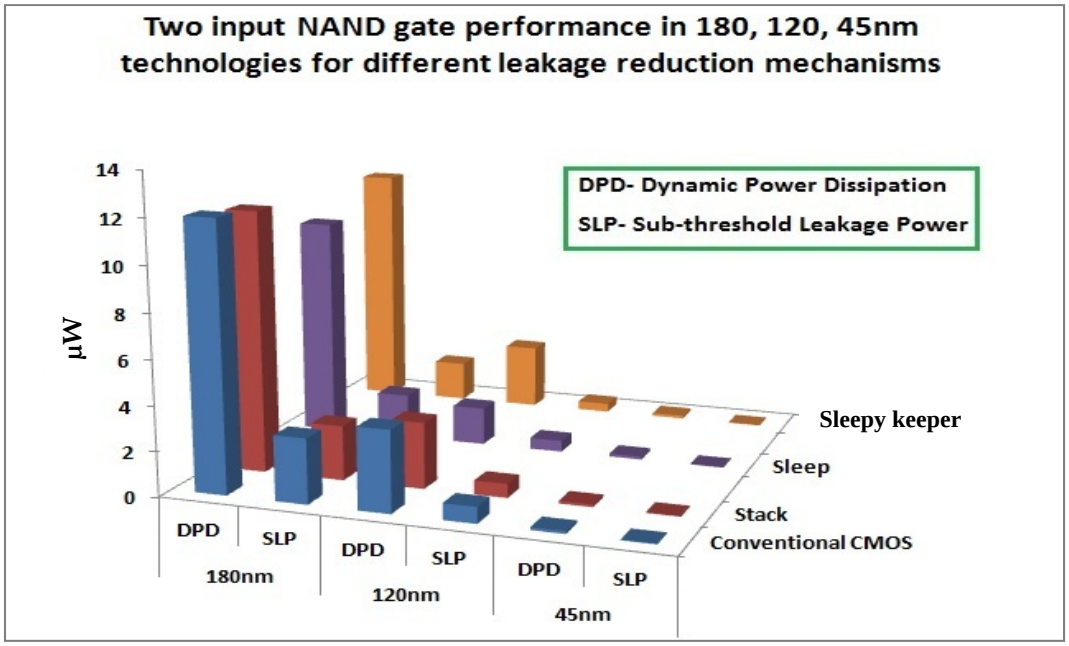

Figure 11. Two input NAND gate performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

Table 3 compares the performance of a half adder in 180, 120 and 45 nm technologies with different leakage reduction mechanisms applied on a conventional CMOS Half adder and is depicted in Fig. 12.

Table 3. Half adder performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

Technology	180nm		120nm		45nm	
Technique	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)	Dynamic Power Dissipation (µW)	Subthreshold Leakage Power (µW)
Conventional CMOS	15.644	4.23	6.740	0.912	0.726	0.103
Stack	14.232	3.87	5.359	0.851	0.699	0.101
Sleep	12.047	2.789	4.820	0.702	0.796	0.092
Sleep Keeper	13.879	2.3	5.024	0.589	0.912	0.073

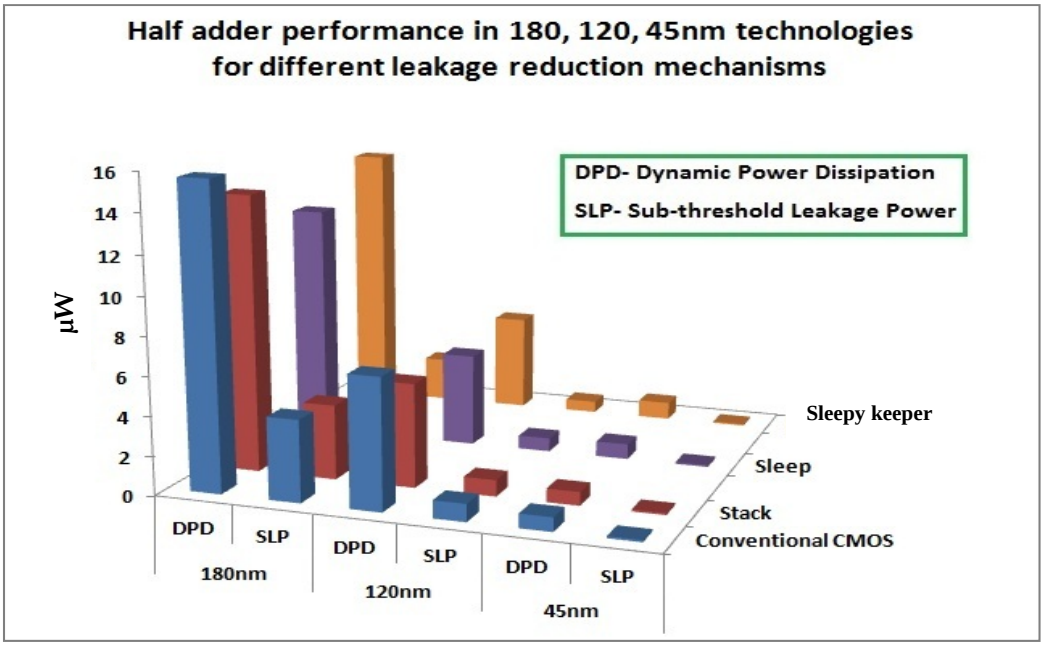

Figure 12. Half adder performance in 180, 120, 45nm technologies for different leakage reduction mechanisms.

From tables Table 1-3, it can be observed that the sub-threshold leakage power has been reduced with sleepy keeper technique compared with the other leakage reduction mechanisms for the digital CMOS circuits like inverter, a two input NAND gate and a Half adder. But the dynamic power dissipation associated with that technique is increased due to additional high threshold voltage transistors. However, when static dissipation reduction is required according to the application, the sleepy keeper technique is preferred over other techniques. In deep sub-micron and nanoscale technologies, this technique can be utilized for designing digital circuits with improvement in the overall static power dissipation, which is mainly due to sub-threshold leakage power dissipation. As the technology node is reduced to 45nm technology, the power dissipation has reduced when compared to other technologies like 120, 180 nm. The sleepy keeper technique is thus advantageous in static power reduction along with preserving the state.

5. Conclusion

The performance of inverter, two-input NAND gate, and half adder digital circuits were studied for sub-threshold power leakage. Even though each and every leakage reduction mechanism has its own advantages and disadvantages, choosing a leakage reduction mechanism depends on the type of circuit and end user application. In this paper, the sleepy keeper approach was found to be the best leakage reduction mechanism for several digital circuits compared to stack and sleep approaches. The sleepy keeper approach resulted in a sub-threshold power leakage of 38%, 42.2%, and 61% for 180nm, 120nm, and 45nm technologies, respectively, for inverters. For a two-input NAND gate, the reduction in subthreshold leakage current was 38.3%, 46.9%, and 36.6% for 180nm, 120nm, and 45nm technologies, respectively. The sleepy keeper approach resulted in a sub-threshold leakage reduction of 45.6%, 35.4%, and 29.1% for 180 nm, 120 nm, and 45 nm technologies, respectively, for half adders.

References

Boray S, Deepak S, Nunez A (2007), Analysis of subthreshold leakage reduction in CMOS digital circuits. *50th Midwest Symposium on Circuits and Systems* 1400-1404.

Borkar S (1999), Design challenges of technology scaling. *IEEE Micro Journal* 19(4): 23-29.

Bursky D (1995), Power reduction schemes promise cool digital ICs. *Electronic Design Journal* 43(1): 51.

Johnson MC, Somasekhar D, Roy K (2002), Leakage control with efficient use of transistor stacks in single threshold CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 10(1).

Manish K, Md Anwar Hussain, Sajal KP (2012), Performance of a two input NAND gate using subthreshold leakage control techniques. *Journal of Electron Devices* 14: 1161-1169.

Roy K, Mukhopadhyay S, Mahmoodi MH (2003), Leakage current mechanisms and leakage reduction techniques in deep sub micrometer CMOS circuits. Proceedings of the IEEE 91(2): 305-327.

Saini P, Mishra R (2012), Leakage power reduction in CMOS circuits. *International Journal of Computer Applications* 55(8): 42-48.

Se HK, Mooney VJ (2006), Sleepy keeper: a new approach to low-leakage power VLSI design. *International Conference on Very Large Scale Integration* 367-372.