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High-Performance BiCMOS Transimpedance Amplifiers for Fiber-Optic Receivers

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مضخمات BiCOMS Transimpadence ذات مواصفات عالية لأجهزة استقبال عبر الاسلاك الضوئية

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االخلاصة: تم تصميم مضخات **Transimpadence** جديدة تعتمد على تكنولوجيا **BiCOMS** ذو القاعدة المشتركة وذلك لاجهزة استقبال عبر الاسلاك الضوئية. وكانت الطريقة الجديدة للتصميم والتي تسمي **" A more FET-approach"** قد أضافت بعدا جديدا لكيفية التعامل بصفة أنجح مع المتضادات الطبيعية في تلك المضخمات. وباستخدام تكنولوجيا السليكون **0.8µm** تم عرض نتائج المحاكاة لخصائص أداء مضخمات **total-FET** تشتغل على تردد **7.2GHz** والتي هي قريبة من القيمة القصوى للتكنولوجيا المستعملة **12GHz**. كانت النتائج المتحصل عليها تفوق نتائج ابحاث اخرى حديثة لنفس التكنولوجيا ومتقاربة مع أخرى تستخدم تكنولوجيا **GaAs** التي هي اسرع ولكن مكلفة اكثر. كما انة تم عرض تحليل موسع لتلك التصميمات الجديدة مع مناقشة كيفية تاثير الاقتراب من تصميم يعتمد كليا على **FET** على خصائص الاداء للمضخمات.

المفردات المفتاحية: جهاز استقبال ضوئي، مضخم **BiCOMS Transimpadence**، تكنولوجيا السليكون **0.8µm**، مضخم يستهلك قدرة ضعيفة.

Abstract: High gain, wide bandwidth, low noise, and low-power transimpedance amplifiers based on new BiCMOS common-base topologies have been designed for fiber-optic receivers. In particular a design approach, hereafter called "A more-FET approach", added a new dimension to effectively optimize performance tradeoffs inherent in such circuits. Using conventional silicon 0.8 µm process parameters, simulated performance features of a total-FET transimpedance amplifier operating at 7.2 GHz, which is close to the technology f_T of 12 GHz, are presented. The results are superior to those of similar recent designs and comparable to IC designs using GaAs technology. A detailed analysis of the design architecture, including a discussion on the effects of moving toward more FET-based designs is presented.

Keywords: Optical receiver, Transimpedance BiCMOS amplifier, 0.8µm silicon technology, Low power amplifier

1. Introduction

Amplifiers for fiber-optic receivers require very high performance features in order to achieve the high gain, wideband, low noise characteristics required for optical communication systems. Some very elegant called "current-mode" optical transimpedance amplifiers (TIAs) using BiCMOS process have been reported (Halkias et al., 2000; Vansiri and Toumazou, 1995; Toumazou and Park, 1996). These TIAs are based on a common-base (CB) architecture, employing current shunt feedback. Two main advantages of the current-mode approach are the very wide bandwidth and the low-input resistance of the circuit. This renders the amplifier bandwidth insensitive to the capacitance of the pin photodiode at the input. In pin photodiode receivers, the TIA has to achieve wide band width, low noise, high and accurate gain, and low power consumption. However, these requirements conflict with each other, requiring tradeoffs to be made to suit a particular application. A current mode CB configuration has the potential to achieve simultaneously high bandwidth and high feedback resistors, potentially improving the amplifier gain and noise performance (Vansiri and Toumazou, 1995; Toumazou and Park, 1996; Ikeda *et al*. 2001).

In this paper, new design approaches of BiCMOS-CB TIAs in a current-feedback configuration for high-speed optical communication applications are presented. The TIAs are design optimized for implementation with a standard, commercially available, 0.8-µm BiCMOS technology. A detailed analysis on the effect of moving toward a more-FET based design is presented. The results are compared to recent similar designs.

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2. Quantitative Description of Architecture

The new CB topologies are shown in Figs. 1 and 2 (design 1 and 2), respectively. The basic architecture consists of a CB input stage Q_1 followed by a common-source amplifier stage M_2, and Q_2 and Q_3 are buffers. Another CB design reported in (Toumazou and Park, 1996) is also shown in Fig. 3 for comparison.

What is special about the new designs compared to previous CB schemes is that it is a total or quasi-FET based approach. That is, solely FETs are used to bias the amplification stages (Q_1 and M_2). In the present designs (1 and 2), FET current mirrors are used to bias stages, where the initial current source of 5 mA must be very stable against external factors (temperature, biasing). Therefore, bandgap reference-based techniques must be used to implement that 5-mA current source. Also, the feedback resistor is connected from the output of Q_2 via R_f to the input of M_2 and not to the emitter of Q_1 (*ie*. the amplifier input), as would be the conventional case. As a result, two straightforward advantages emerge: 1) the total power consumption is lower for the same gain and 2) these FETs should be sized in such a way to increase the gain while optimizing noise performance of the amplifier. This constitutes a new dimension added to optimize performance tradeoffs inherent in such designs while maintaining device processing yield high.

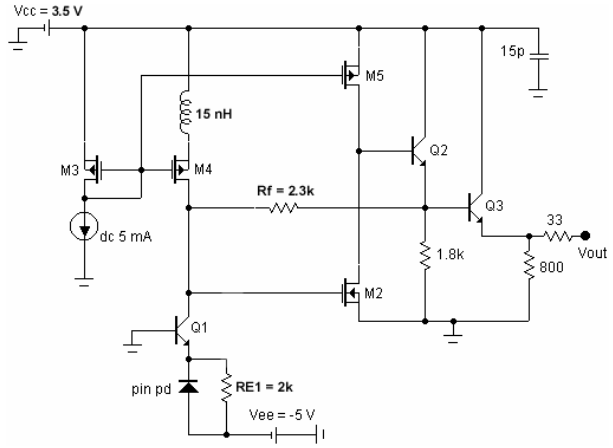

Figure 1. BiCMOS CB TIA (design 1)

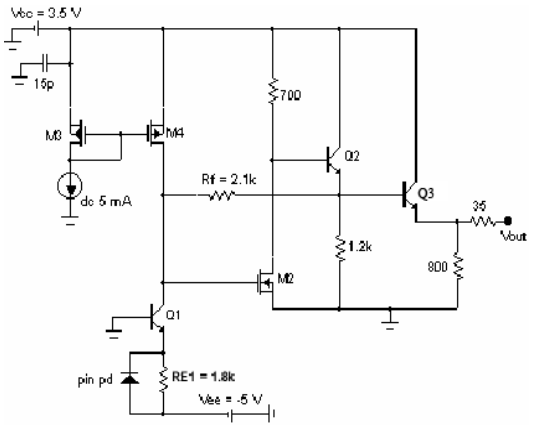

Figure 2. BiCMOS CB TIA (design 2)

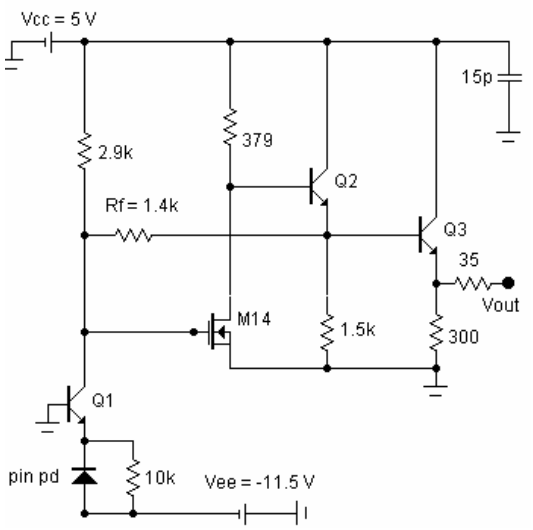

Figure 3. BiCMOS common-base TIA (design 3) (Toumazou and Park, 1996)

The input transistor is a bipolar transistor. Therefore, the collector bias current required is less than the drain bias current required in a common-gate configuration for the same transconductance g_m, hence leading to a lower-power consumption. Alternatively, for the same supply voltage the transconductance g_m is higher in the bipolar transistor case and hence the noise contribution is lower. The amplifier stage is selected to be an FET (M_2) because the input current noise is less than that of a bipolar transistor and because the optimum size can be selected.

Going from design 3 via 2 to 1, the circuit becomes more and more FET-based. We will see what impact this would have on performance features.

3. DC Analysis

The accurate prediction of the DC operating point of such circuits is of critical importance because the various stages are bias interdependent. Extensive DC analysis and optimization of the new CB design circuits was performed. The resistive shunt-feedback reduces the circuit sensitivity to external factors such as biasing, process tolerances, and temperature. Also, the BJT at the input stage gives a higher transconductance for the same supply voltage as explained above, resulting in two main advantages: 1) a higher transimpedance gain (hence low noise) and 2) a low input impedance (almost $1/g_{m1}$). The main objective to accommodate a low DC power consumption, a high transimpedance gain, low-noise, and to insure bias insensitivity within a relatively large range of supply voltages has been successively met. The positive and negative supply voltages V_{cc} and V_{ee} (in Figs. 1 and 2) can be varied within the range from +3.0 to 6.0 V and from -5.8 to -4.6 V, respectively, without degrading performance. The total DC power consumption (no load) for design 1, 2, and 3 is 56.6, 51.8, and 72.3 mW, respectively. This indicates that the new designs (1 and 2) are better optimized for low power consumption.

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4. AC Analysis

The common-base topology adopted makes the -3 dB bandwidth of the amplifier totally independent of the photodiode input capacitance, which determines only a non-dominant pole since the input resistance of M_1 is small (Toumazou and Park, 1996).

Figure 4 shows the small signal hybrid π model of the common-base transimpedance amplifier of Fig. 2 at high frequency.

Here the base spreading resistances of bipolar junction transistors were neglected. The transfer function of this amplifier is governed by five major time constants: at the input (tin), associated with the Miller feedback resistance at the input of M_2 (t_{RfMin}), associated with the Miller feedback resistance at the output of M_2 (t_{RfMout}), associated with the base-emitter capacitance of Q_2 (t_{Cbe2}), and at the output (t_{out}). Let us assume that tRfMin is the dominant time constant (which often has a much lower value) when compared to the other time constants. Therefore, the -3 dB bandwidth of the amplifier is approximately determined by the cut-off frequency as:

$$f_{-3dB} \cong \frac{1}{2\pi t_{R_{fMin}}} \tag{1}$$

where: $t_{R_{fMin}} = R_{Min} C_T$ with $R_{Min} = \frac{R_f}{1 + A_{v2}}$. A_{v2} is the voltage gain of M_2 and $C_T = C_{\mu 1} + C_{gd4} + C_{gs2} + C_{Min2}$. The capacitance C_{i1} is the base-to-collector capacitance of Q_1, C_{gs2} and C_{gd2} are the gate-to-source and gate-to-drain capacitances of M_2, C_{gd4} is the gate-to-drain capacitance of M_4, and C_{Min2} is the Miller capacitance of the gate-to-drain capacitance C_{gd2} of M_2 at its input and given by $C_{Min2} = (1 + A_{v2}) C_{gd2}$.

Therefore, by combining all the above equations Eq. (1) becomes:

$$f_{-3dB} \cong \frac{(1 + A_{v2})}{2\pi C_T R_f} \tag{2}$$

The dominant pole of the amplifier, which determines the -3 dB bandwidth, depends mainly on the input capacitance of M_2 with Miller effect, the input capacitance of Q_1, the drain capacitance of M_4, and the feedback resistor R_f. Since M_2 is a much smaller device, its net input capacitance is small and hence R_f can be made larger for the same equivalent bandwidth, which would result in a lower overall noise. However, smaller device means higher resistance which would reduce the bandwidth. This would impose a careful sizing of M_2 when dealing with the tradeoff between low noise and wide bandwidth. On the other hand, M_4 should be made narrow in order to reduce its noise contribution while preserving adequate bias collector current for Q_1. In Fig. 1, the size of M_5, load of M_2, can be selected to optimize A_{v2} for wide bandwidth.

A critical aspect of the design phase was the optimization of the feedback resistor R_f as well as the size of the FET transistors in a tradeoff between gain, bandwidth, noise, and DC power consumption.

It was shown (Abidi, 1988) that optimum noise performance may be obtained in transimpedance amplifiers employing submicron FET input stages by choosing the width of the input device such that its gate capacitance is one-fifth of the sum of the photodiode and stray capacitance. Based on this criterion, it was concluded that for design 1 (design 2), the optimum value of R_f = 2.3 kΩ (R_f = 2.1 kΩ) and W_2 = 30 μm (W_2 = 30 μm) for L = 0.8 ?m allow the desired transimpedance gain, minimum input noise current density, and low power consumption over the bandwidth of DC-7.2 GHz (4.4 GHz) to be achieved. This was obtained through successive cycles of DC and RF simulations.

Simulated results of transimpedance gain of the new designs (1 and 2) are shown in Fig. 5. Also shown for comparison, the curve reported in (Toumazou and Park, 1996) (design 3). State-of-the-art 12 GHz f_T silicon BiCMOS parts of a conventional 0.8-μm BiCMOS technology were used. It can be seen that going toward a more FET-based configuration (*ie*. from design 3 via 2 to 1), the transimpedance gain as well as the -3 dB bandwidth improves. This trend is more prominent when one compares design 1 (thick solid line in Fig. 5) with design 3 (fine thin solid line in Fig. 5). This can be accounted for by the increasingly higher feedback resistor R_f = 1.4kΩ, 2.1kΩ, and 2.3kΩ which was achieved for design 3, 2, and 1, respectively. This would lead to a lower thermal noise contribution from the feedback resistor. This high transimpedance gain is also due to using more and more active loads from design 3 to design 1 instead of resistive loads, since the closed-loop gain depends on R_f and the open-loop gain.

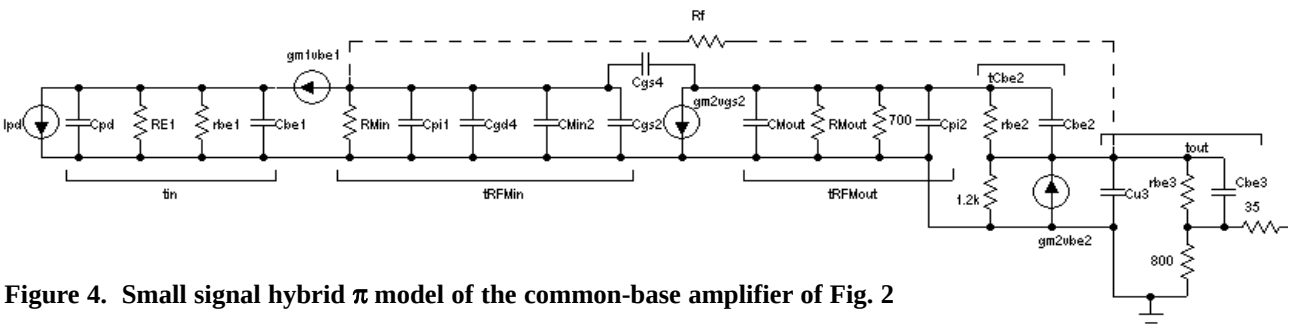

Figure 4. Small signal hybrid π model of the common-base amplifier of Fig. 2

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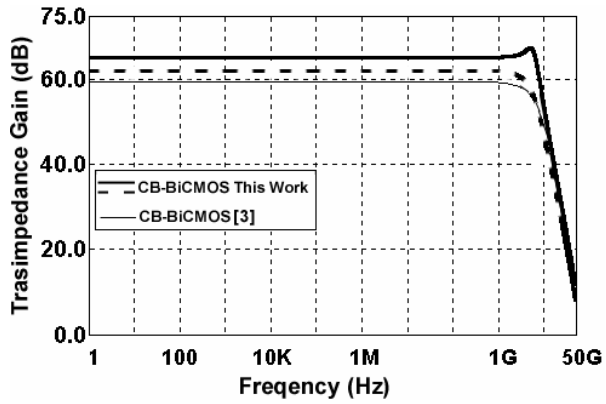

Figure 5. Transimpedance gain versus frequency

5. Noise Analysis

The noise model, used to calculate the noise components, combines the conventional FET rms noise theory with the optical preamplifier (OEIC) noise theory (Minasian, 1987; Smith and Personick, 1980). The total input-referred equivalent noise current spectral density of designs 1 and 2 is approximately given by:

$$S_{eq}(f)=\frac{4kT}{R_f}+\frac{4kT}{R_{E1}}+4kTr_{bb1}\left[\frac{1}{R_{E1}^2}+(2\pi f)^2(C_d)^2\right]$$
$$+\frac{2kT}{r_{be1}}+\frac{2kTr_{be1}}{\beta_1}\left[\frac{1}{R_{E1}^2}+(2\pi f)^2(C_d+C_{be1})^2\right]+2qI_{g2}$$
$$+\frac{4kT\Gamma}{g_{m2}}\left[\frac{1}{R_f^2}+(2\pi f)^2(C_{gs2}+C_{\mu 1}+C_{gd4})^2\right] \qquad (3)$$
$$+\frac{g_{m4}r_{be1}}{\beta_1}\frac{2kTr_{be1}}{\beta_1}\left[\frac{1}{R_{E1}^2}+(2\pi f)^2(C_d+C_{be1})^2\right]$$

In Eq. (3), k is the Boltzmann constant, T is the absolute temperature, r_{bb1} is the base spreading resistance of Q1 (0.3 Ω), C_d is the capacitance of the pin photodiode (0.32 pF which is typical for a pin photodiode), $r_{be1} = kT/qI_{B1}$ with I_{B1} (27 uA) is the base current of Q_1, C_{be1} (0.8 pF) is the base-emitter capacitance of Q_1 and $C_{\mu 1}$ (defined above) = 0.2 pF, β_1 (100) is the ac current gain of Q_1, I_{g2} is the gate leakage current of M_2, C_{gs2} = 1.0 pF, C_{gd2} = C_{gd4} = 0.3 pF, g_{m2} = 7.0 mS, g_{m4} = 15.0 mS, q is the electron charge, Γ is the excess noise factor equal to 1.7 (Abidi, 1988) to account for the short-channel effects. The first three terms in Eq. (3) represent thermal noise contributions by R_f, R_{E1}, and r_{bb1}, respectively. The next two terms are base and collector shot noise current of Q_1, the sixth term is noise contribution by gate leakage current of M_2, which can be neglected (Halkias *et al*. 2000). The last two terms represent the channel thermal noises of M_2 and M_4, respectively.

Figure 6 shows simulated results of the total rms input-referred noise current of the new designs, as calculated using Eq. (3) over a bandwidth of 10 GHz. Also shown for comparison, the results reported in (Toumazou and Park, 1996) (design 3).

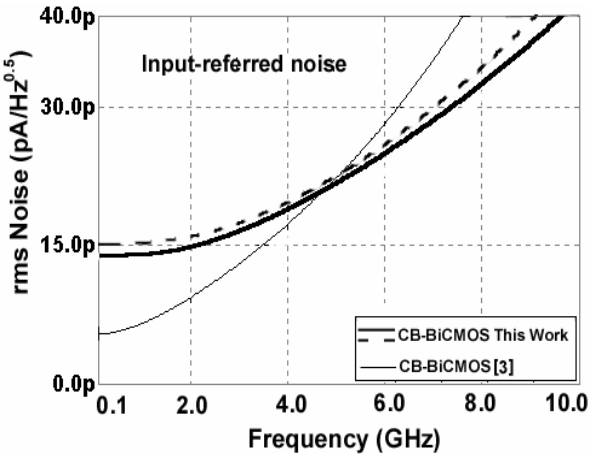

Figure 6. Total mean input-referred noise current versus frequency

State-of-the-art 12 GHz f_T silicon BiCMOS parts of a conventional 0.8 μm BiCMOS technology have been used. Two important features are clear. First, above around 5.0 GHz the new designs offer a lower total noise performance compared to that of (Toumazou and Park, 1996), whereas the opposite occurs otherwise. Second, Moving toward higher frequencies, the noise current becomes increasingly lower when we move toward a more FET-based design (solid line). This is important since the lower noise at higher frequencies offered by the total-FET based design will result in a lower BER at high data rates.

Preliminary results showed that the addition of the inductor L = 2-15 nH (realizable monolithically as transmission lines) as shown in Fig. 1 results in a significant noise reduction. This can be explained by the reduction of noise contribution of M_4 (last term in Eq. (3)) by adding the inductor. M_4 noise spectral density with the inductor becomes:

$$\frac{g_{m4}}{\sqrt{1+(g_{m4}2\pi fL)^2}}\frac{r_{be1}}{\beta_1}\frac{2kTr_{be1}}{\beta_1}\left[\frac{1}{R_{E1}^2}+(2\pi f)^2(C_d+C_{be1})^2\right] \qquad (4)$$

From Eq. (4), with g_{m4} = 30 mS, and L = 15 nH, the inductor will reduce the noise spectral density of M_4 by a factor of 1/3 at 1 GHz.

Table 1 summarizes performance features of the new CB designs (1 and 2) and those of (Toumazou and Park, 1996).

It is clear that the results obtained with the new CB designs are superior to those reported in (Toumazou and Park, 1996) and in (Park and Yoo, 2003). Also, these results are better than those reported in (Haralabidis et al., 2000) and fairly approach those obtained with GaAs MESFET and InP-HBT (Huber *et al*. 2000; Yoneyama *et a*l. 2000; Minasian, 1987).

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Table 1. BiCMOS CB TIA design parameters

	Gain (dB)	BW (GHz)	Noise (pA/Hz$^{0.5}$) @ 3.5	7 GHz	Total Power (mW)
New Design 1	65.2	7.2	17.7	28.7	56.6
New Design 2	62.1	4.4	18.3	29.4	51.8
Design 3 [3]	59.8	4.2	15.2	35.5	72.3

Figure 7 shows the transient response of the previous CB TIA designs when driven by a 2.5 Gbps input current pulse train. It can be clearly seen that moving toward a more FET-based design, the output swing widens and the response becomes faster. Although the settling time in this case is bigger, still the response is faster and settles within the time frame of the driving pulses period. For the total-FET based design (thick solid line), the response clearly reaches 200 mV output swing for a 100 μA input current. According to that, one can expect a sufficiently open eye diagram at 2.5 Gbps for NRZ synchronous links.

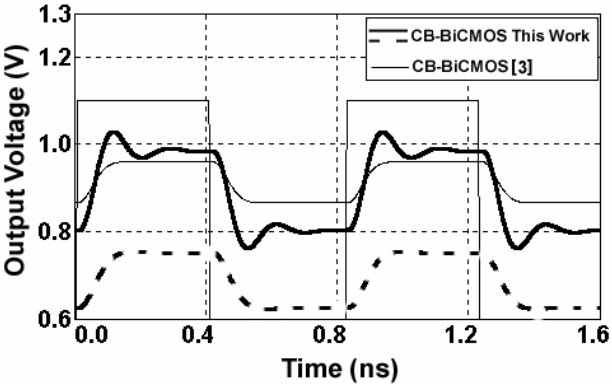

Figure 7. Transient response of the CB BiCMOS TIAs at 2.5 Gbps for a 100μA pulse input current signal

Noise simulations of the new designs have also been conducted using 0.6 μm BiCMOS process parameters. Results showed even lower total rms noise current; more than 1 dB lower in the frequency range above 4.0 GHz. This may indicate the validity of the new design approach for shorter channels also. Further investigations are in order in this regard.

6. Conclusions

High-performance BiCMOS common-base transimpedance amplifiers for fiber-optic receivers have been improved. In particular, a more FET-based approach was found effective in potentially optimizing performance features. Simulated results showed improved transimpedance gain, noise characteristics, bandwidth, and power consumption when compared to recent similar designs. A transimpedance gain as high as 65.2 dB over a bandwidth of 7.2 GHz, which is close to the technology f_T of 12 GHz, was achieved. The 3.5 GHz and 7.0 GHz total equivalent input-referred noise current have been minimized to achieve 17.7 and 28.7 pA/Hz$^{0.5}$, respectively. Also the total power consumption of the circuit was optimized to 56.6 mW. These performance features are fairly comparable to those reported using GaAs MESFET.

While optimizing the design for gain, noise and power, little attention has been given to dynamic range and output swing. However, now that the new approach is demonstrated, much study is aimed at optimizing other performance features.

Acknowledgments

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